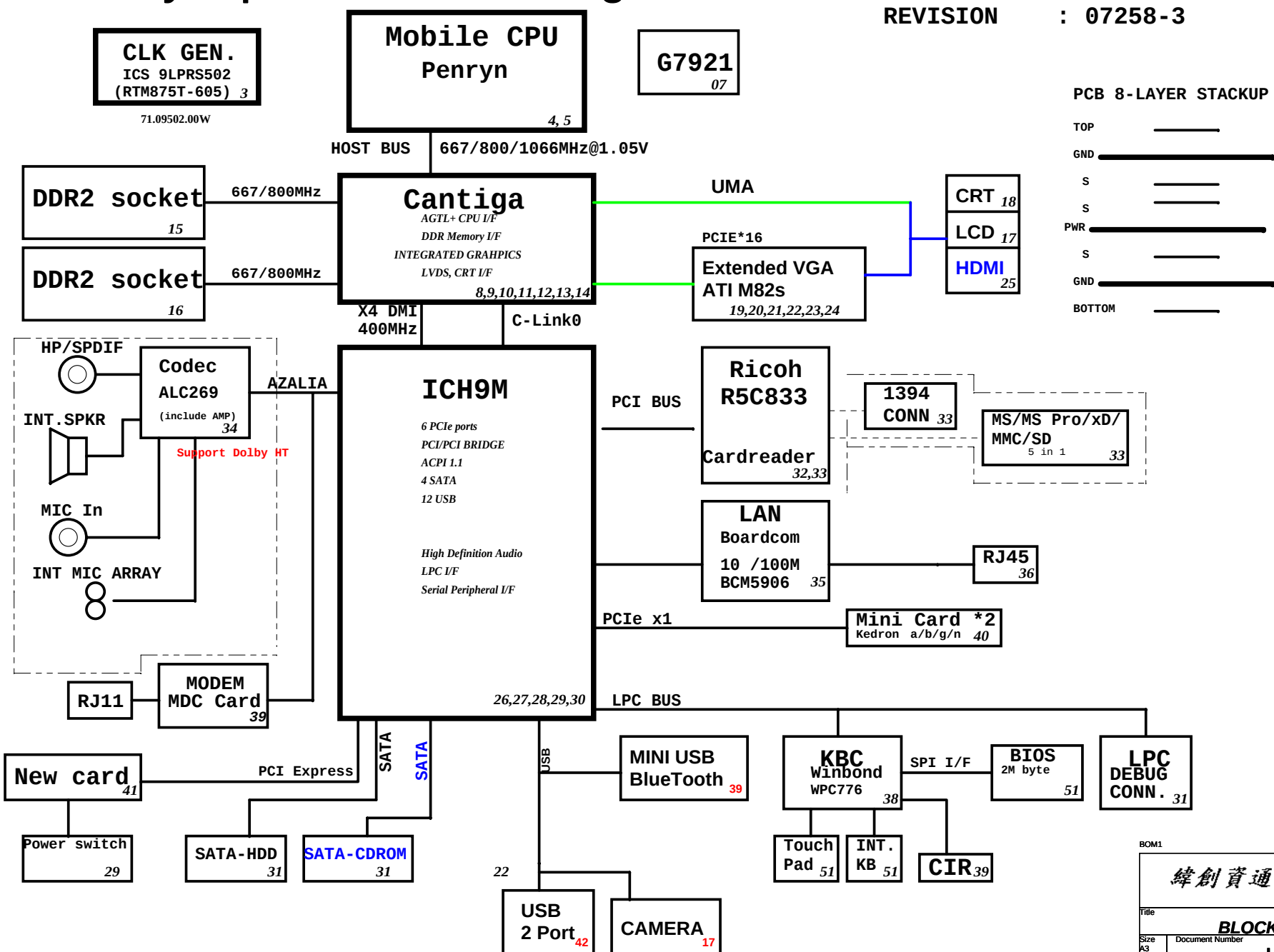


Olympus Block Diagram

Project code: 91.4Y601.001
PCB P/N : 48.4Y603.0SA
REVISION : 07258-3



SYSTEM DC/DC ISL6236 38	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)
SYSTEM DC/DC TPS51124 40	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D5V_S3(10A)
TPS51117 39	
DCBATOUT	1D8V_S3 (2.5A)
TPS51100 39	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5308 39	
3D3V_S0	2D5V_S0 (300mA)
CHARGER BQ24750 42	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC ISL6266A 37	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A
NB DC/DC ISL6263A 41	
INPUTS	OUTPUTS
DCBATOUT	GFX_CORE
SC411 48	
DCBATOUT	1D5V_S3

ICH9M Functional Strap Definitions

ICH9 EDS 642879 Rev.1.5 page 92

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low. When TP3 not pulled low at rising edge of PWROK, sets bit1 of RPC.PC(Config Registers:Offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT4#/GPIO51	ESi Strap (Server Only) Rising Edge of PWROK	ESi compatible mode is for server platforms only. This signal should not be pulled low for desktop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low: Top-Block Swap mode (inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PC1, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode (ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low: the Flash Descriptor Security will be overridden. If high, the security measures will be in effect. This should only be enabled in manufacturing environments using an external pull-up resistor.

ICH9M Integrated Pull-up and Pull-down Resistors

ICH9 EDS 642879 Rev.1.5

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

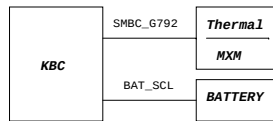
Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Montevina Platform Design guide 22339 0.5 page 218

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1667 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG6 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0 = The iTPM Host Interface is enabled (Note 2) 1 = The iTPM Host Interface is disabled (default)
CFG7	Intel Management Engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIE Graphics Lane	0 = Reverse Lanes, 15->0, 14->1 ect.. 1 = Normal operation (default): Lane Numbered in order
CFG10	PCIE Loopback enable	0 = Enable (Note 3) 1 = Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 01 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation (Default): Lane Numbered in Order 1 = Reverse Lanes DMI x4 mode [MCH -> ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [MCH -> ICH]: (3->0, 2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display Port or PCIE is operational (Default) 1 = Digital Display Port and PCIE are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card Present (Default) 1 = SDVO Card Present
LDDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1 = LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-descriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.

SMBus



USB Table

USB	
Pair	Device
0	Combo (ESATA/USB)
1	NC
2	USB2
3	USB4
4	USB3
5	BLUETOOTH
6	WEBCAM
7	FT
8	MINICARD
9	NEW1

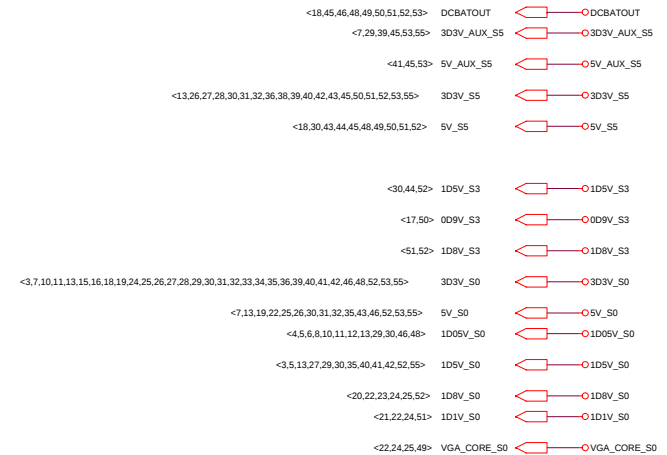
PCI Routing

page 17

	IDSEL	INT	REQ	GNT
TI7412	AD22	6: CARDBUS B: 1394 F: Flash Media G: SD Host	0	0

PCIE Routing

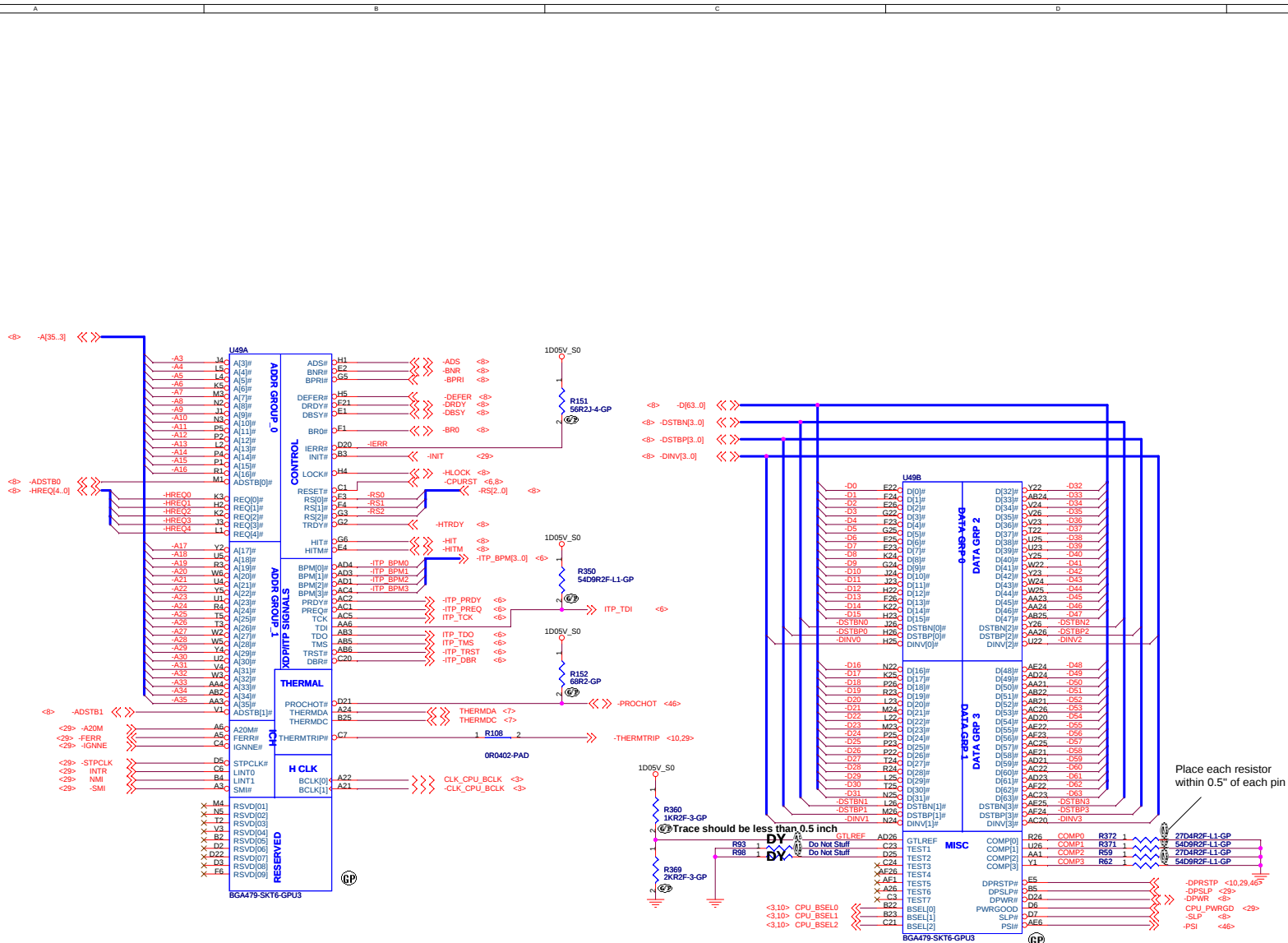
LANE2	MiniCard WLAN
LANE3	NewCard WLAN



ROM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsuehshih,
Taipei Hsien 221, Taiwan, R.O.C.

Reference		
Size C	Document Number	Rev
	LT32M	-3
Date: Monday, July 07, 2008	Sheet 2	of 54



Place each resistor within 0.5" of each pin

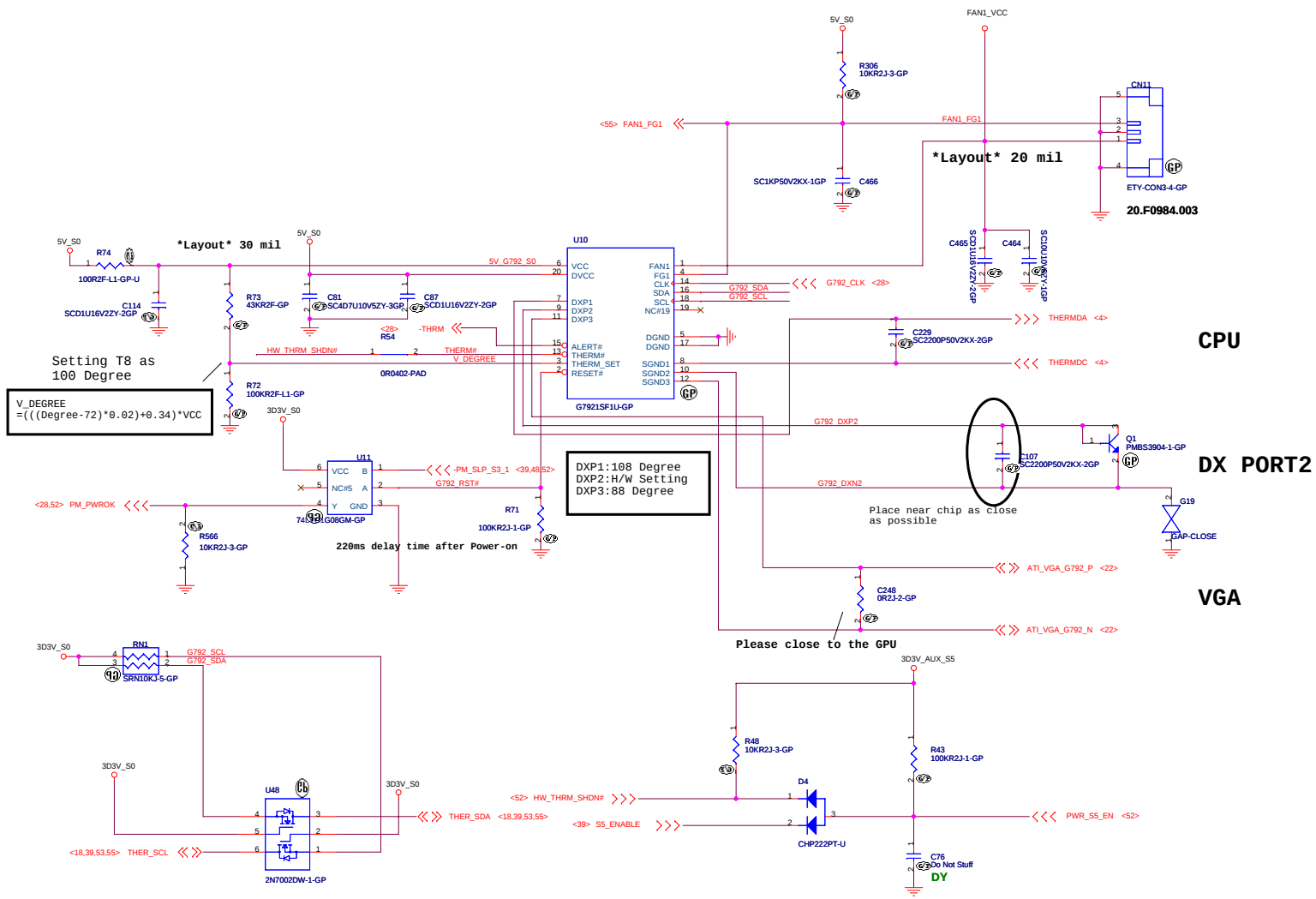
BOML

緯創資通 Wistron Corporation
21F, 8F, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.

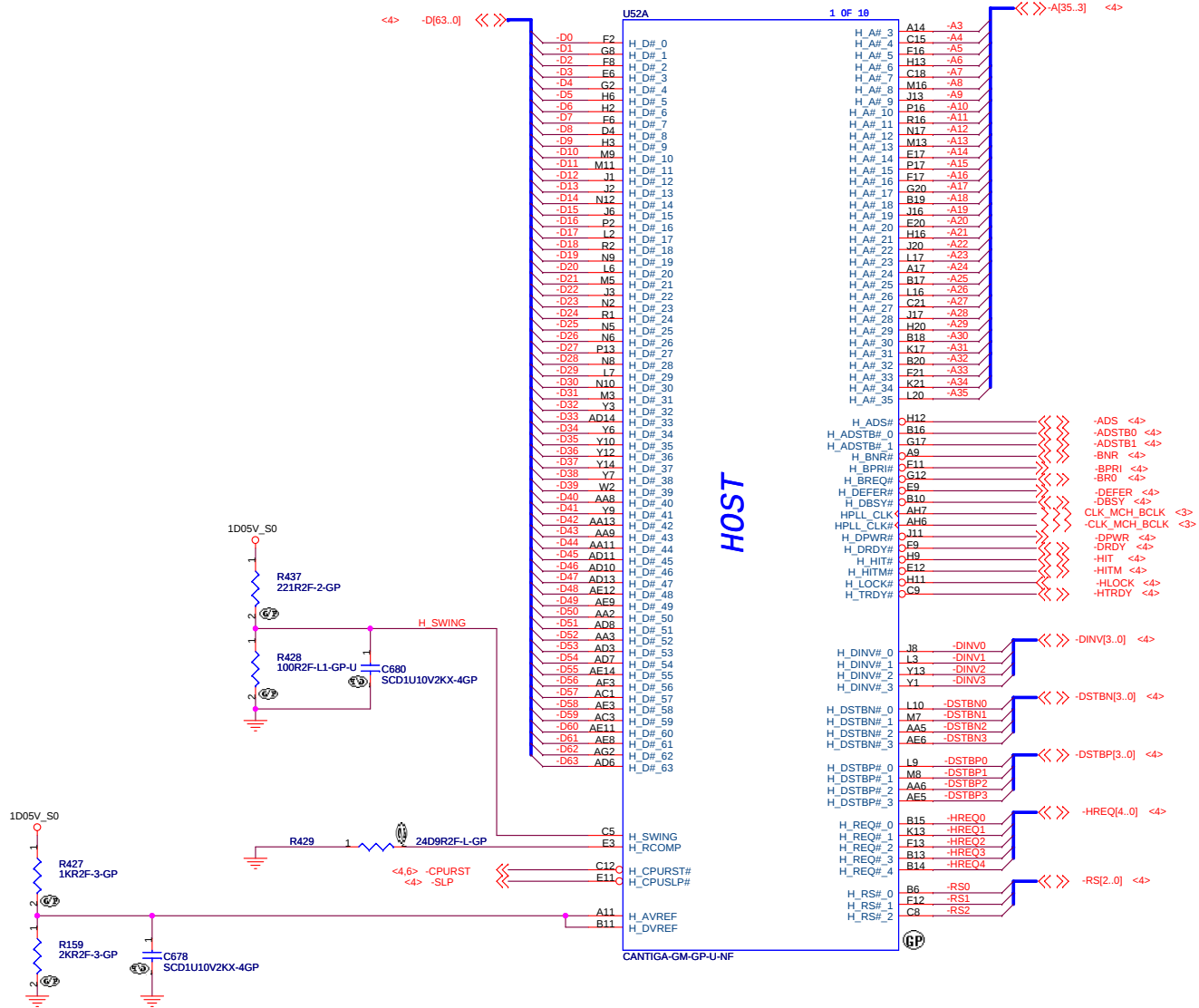
File: **Penryn CPU(1/2)**
Size: **Document Number**
C: **LT32M**
Date: **Monday, July 07, 2008** Sheet **4** of **54**



- | Ref Des | For ITP.XDP |
|---------|-------------------|
| J1 | NO_ASM->ASM |
| C157 | NO_ASM->ASM |
| R140 | NO_ASM->1K 5% ASM |
| R144 | ASM (No Change) |
| R136 | ASM->NO_ASM |
| R145 | ASM (No Change) |
| R141 | ASM->54.9 1% ASM |
| R143 | ASM->54.9 1% ASM |



BOM1

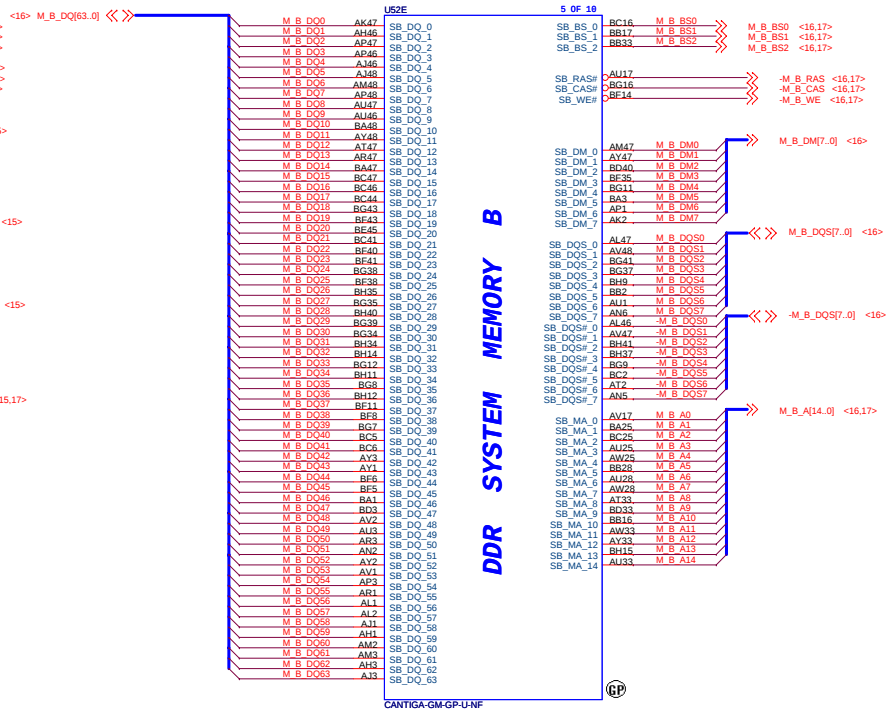
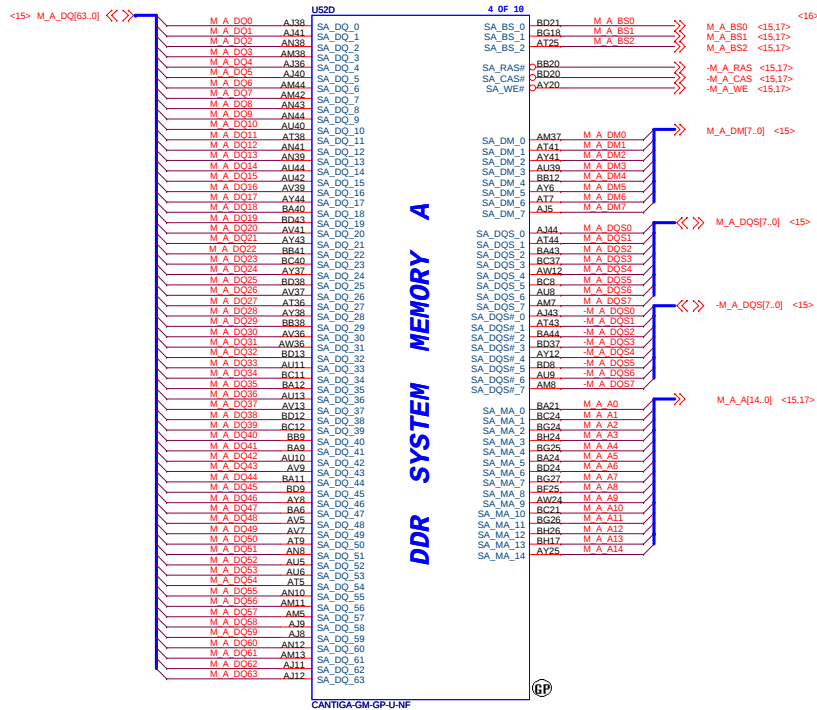


Route H_XSWING & H_YSWING
10 mil wide / 20 mil spacing

Route H_XRCOMP &
H_YRCOMP 10 mil wide /
20 mil spacing

BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Cantiga(17):HOST I/F	
Size A3	Document Number LT32M
Date: Monday, July 07, 2008	
Sheet 8 of 54	
Rev -3	



BOML

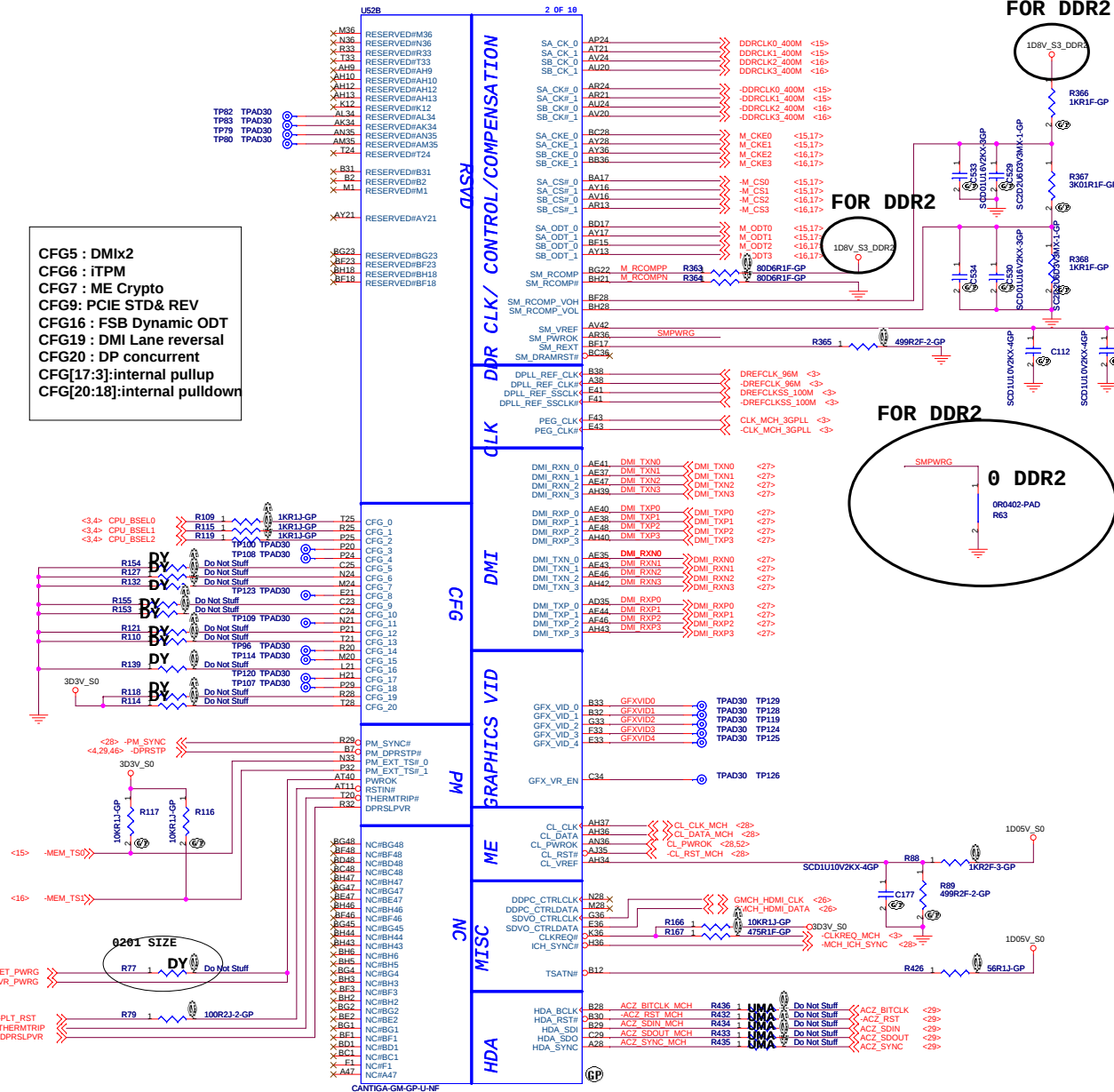
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichien,
Taipei Hsien 221, Taiwan, R.O.C.

File Cantiga(2/7):DDR3
Size C Document Number LT32M Rev -3
Date: Monday, July 07, 2008 Sheet 9 of 54

ME DEBUG PORT PIN OUT TABLE

RESERVED#AL34	ME_JTAG_TCK
RESERVED#AK34	ME_JTAG_TDI
RESERVED#AN35	ME_JTAG_TDO
RESERVED#AM35	ME_JTAG_TMS

CFG5 : DMIx2
 CFG6 : ITPM
 CFG7 : ME Crypto
 CFG9: FSIE STD& REV
 CFG16 : PSB Dynamic ODT
 CFG19 : DMI Lane reversal
 CFG20 : DP concurrent
 CFG[17:3]:internal pullup
 CFG[20:18]:internal pulldown



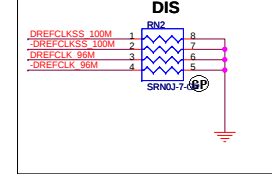
FOR DDR2

FOR DDR2

FOR DDR2

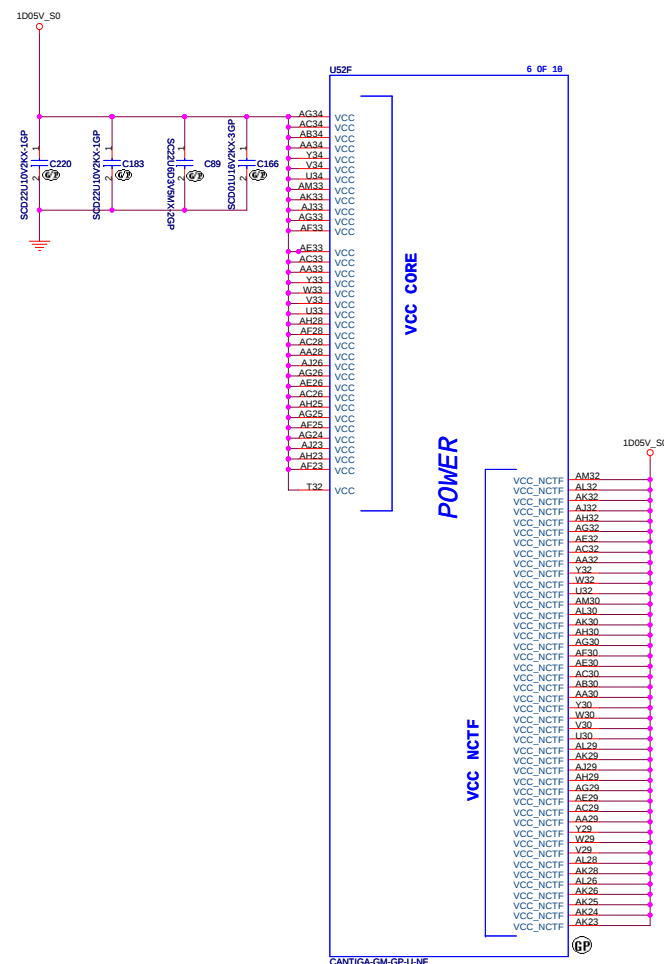
FOR DDR2

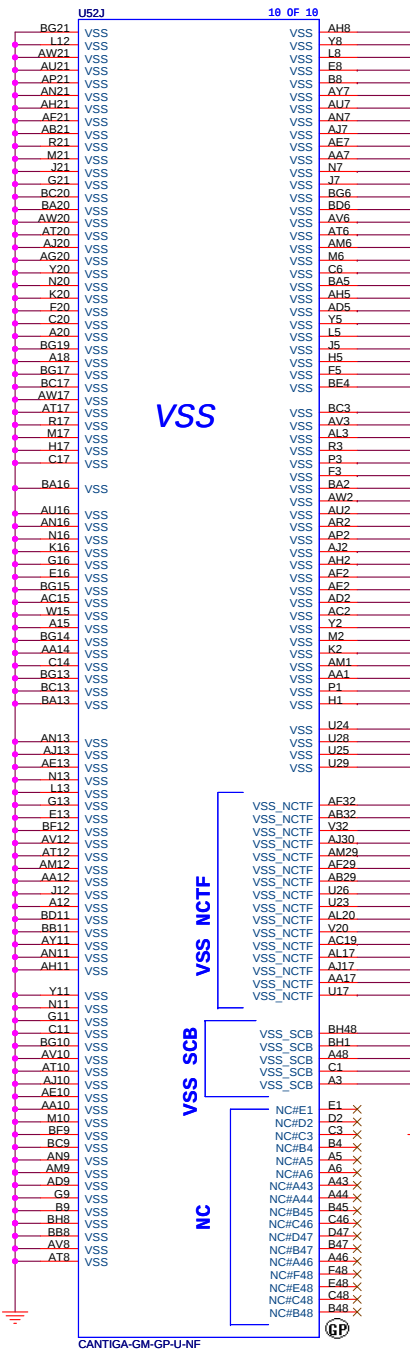
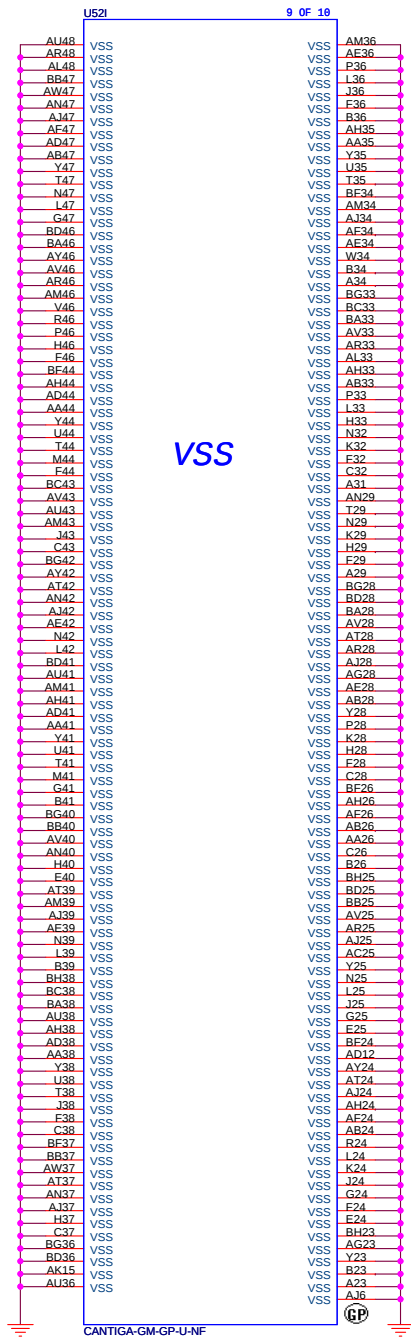
0 DDR2



BOM1

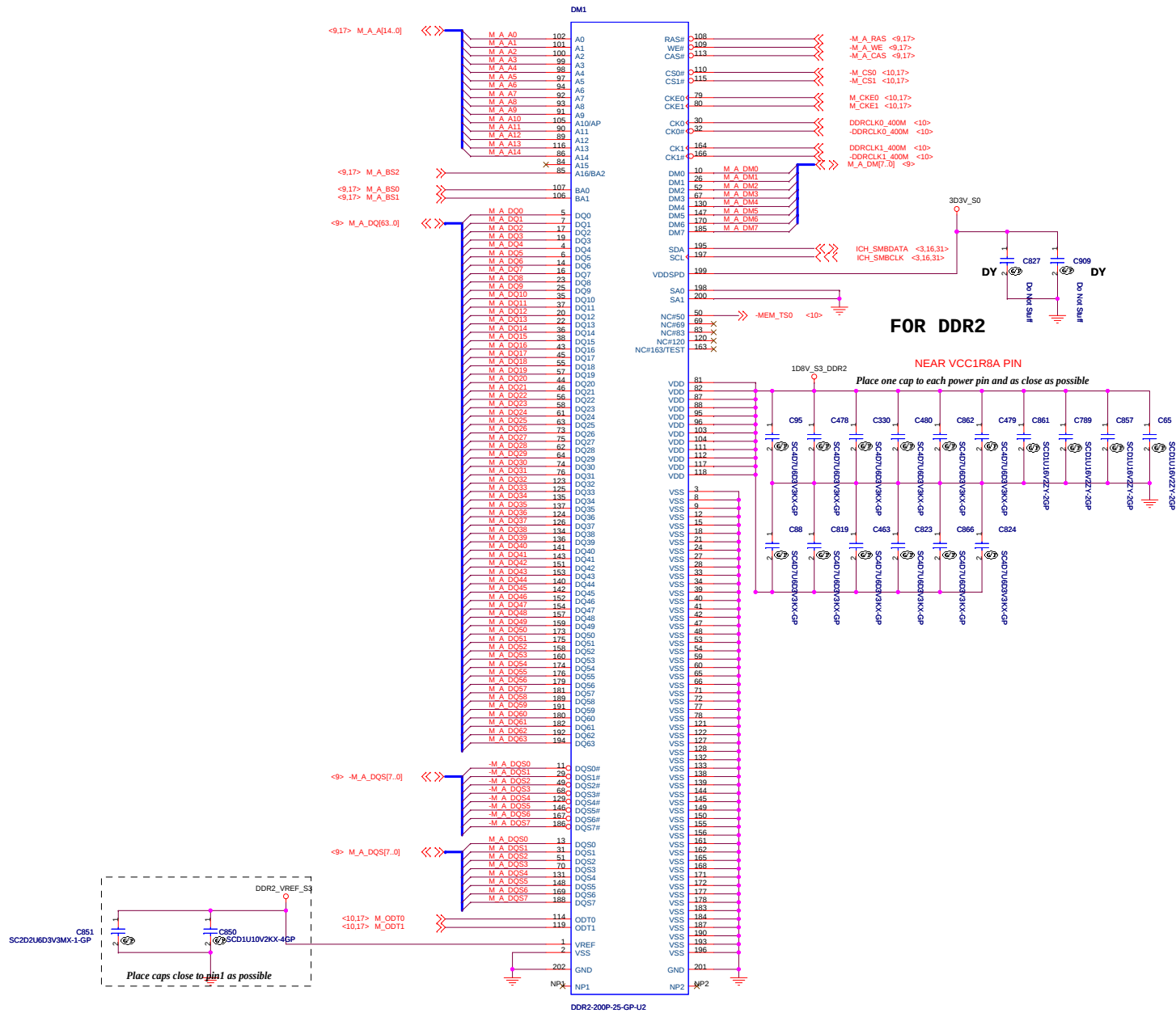
1D8V_S3_DDR2



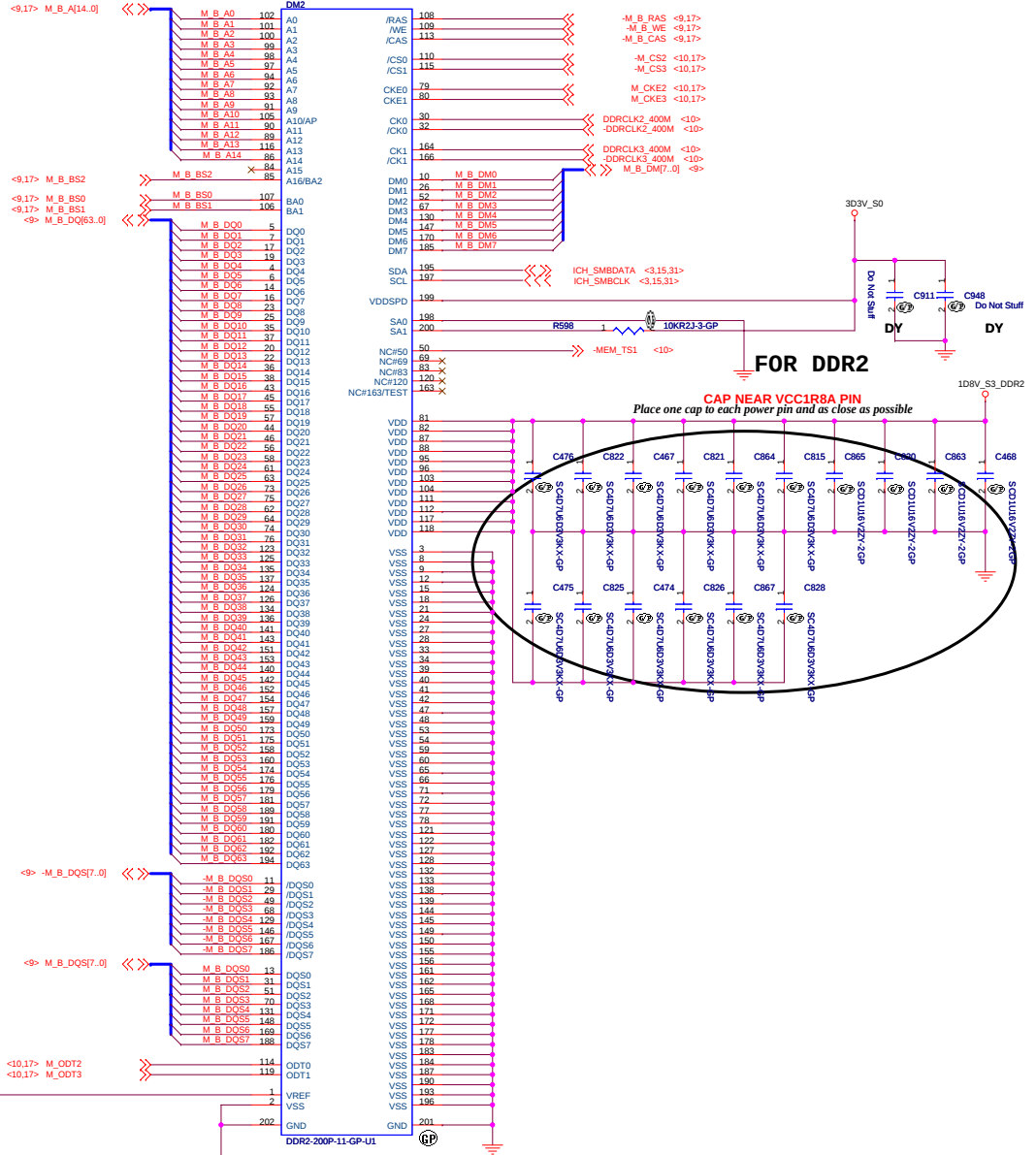


BOM1

緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Cantiga(8/7): GND	
Size	Document Number
A3	LT32M
Date:	Monday, July 07, 2008
Sheet	14 of 54

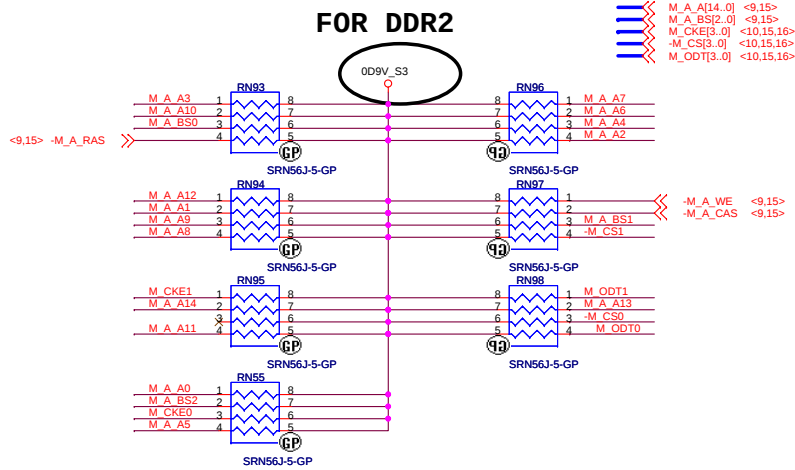


Place near VCC3B Power rail bridge via under SO-DIMM



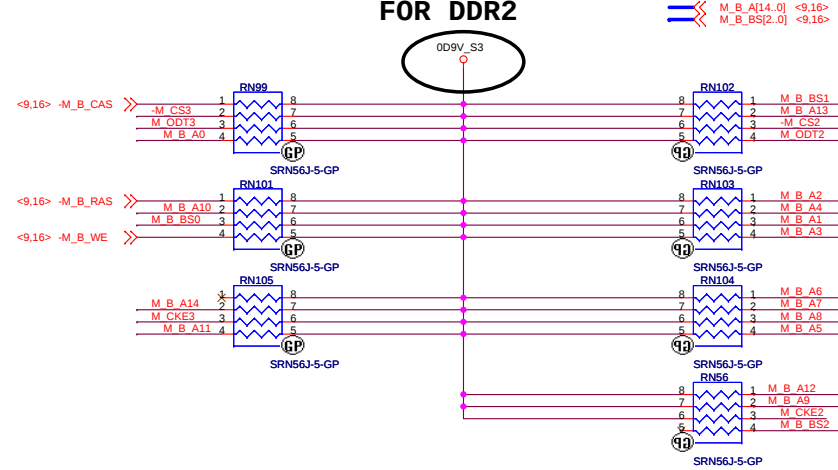
CHANNEL A PARALLEL TERMINATION

FOR DDR2



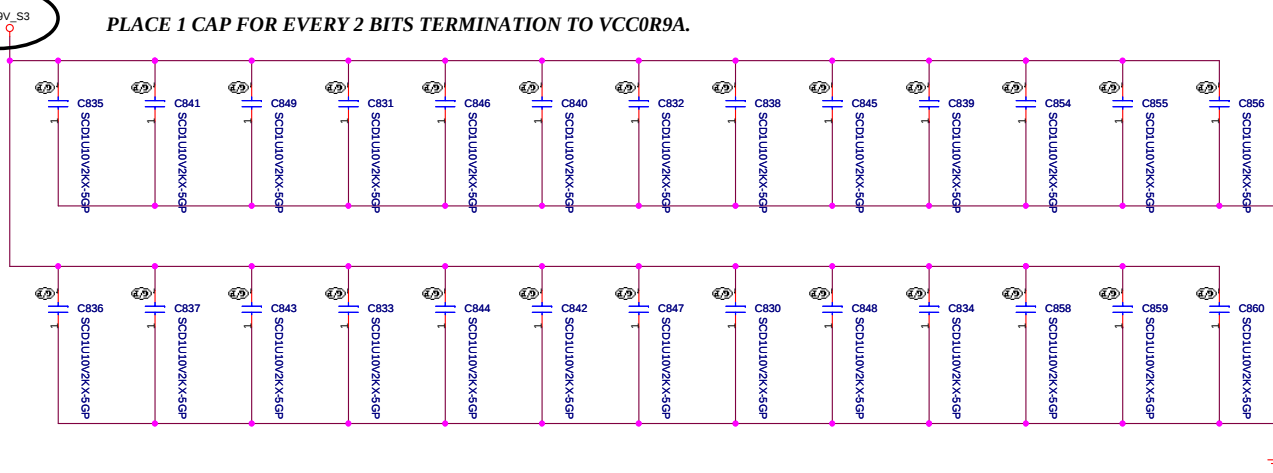
CHANNEL B PARALLEL TERMINATION

FOR DDR2



FOR DDR2

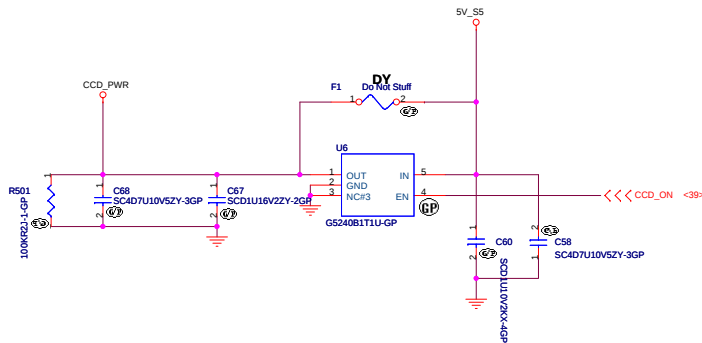
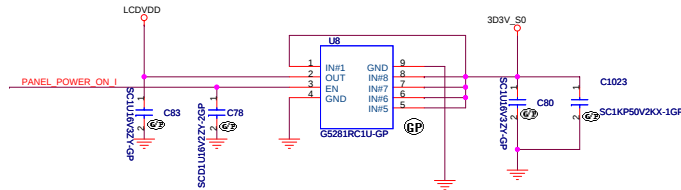
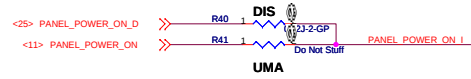
PLACE 1 CAP FOR EVERY 2 BITS TERMINATION TO VCC0R9A.



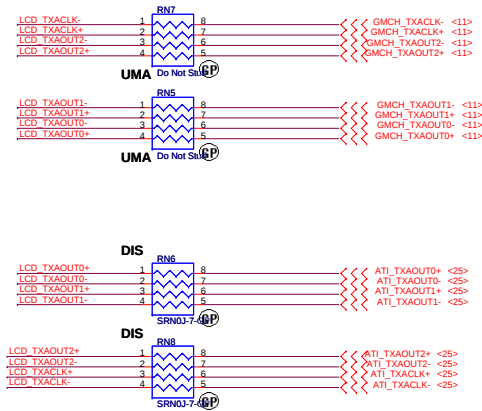
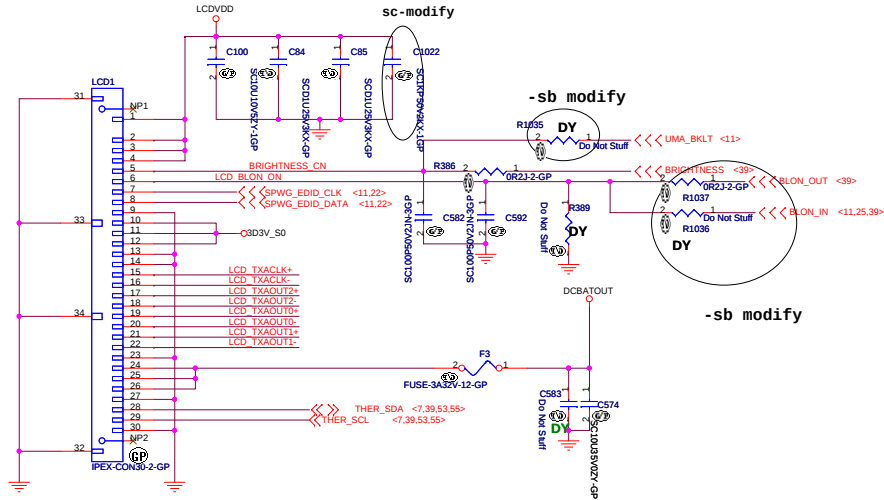
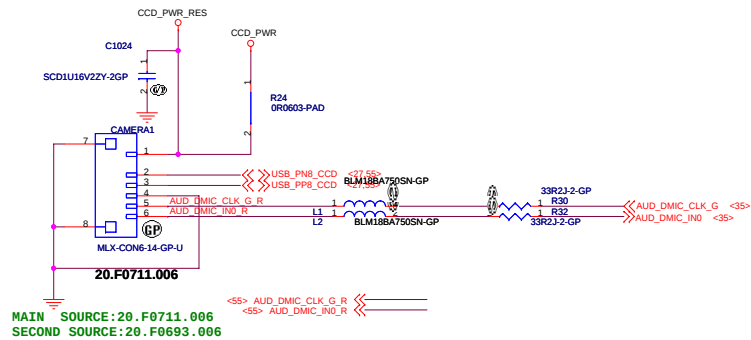
BOM1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
DDR-2 TERMINATION/DECOUPLING			
Size	Document Number	Rev	
Custom	LT32M	-3	
Date:	Monday, July 07, 2008	Sheet	17 of 54

LCD/INVERTER CONN



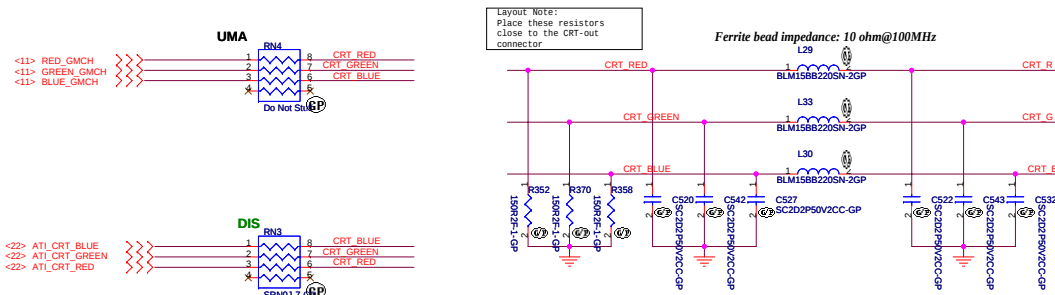
CAMERA & DIG-MIC



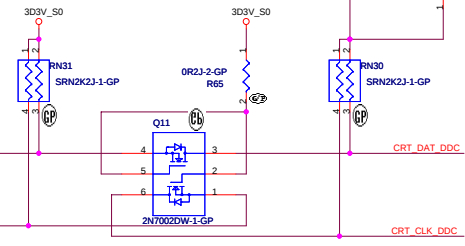
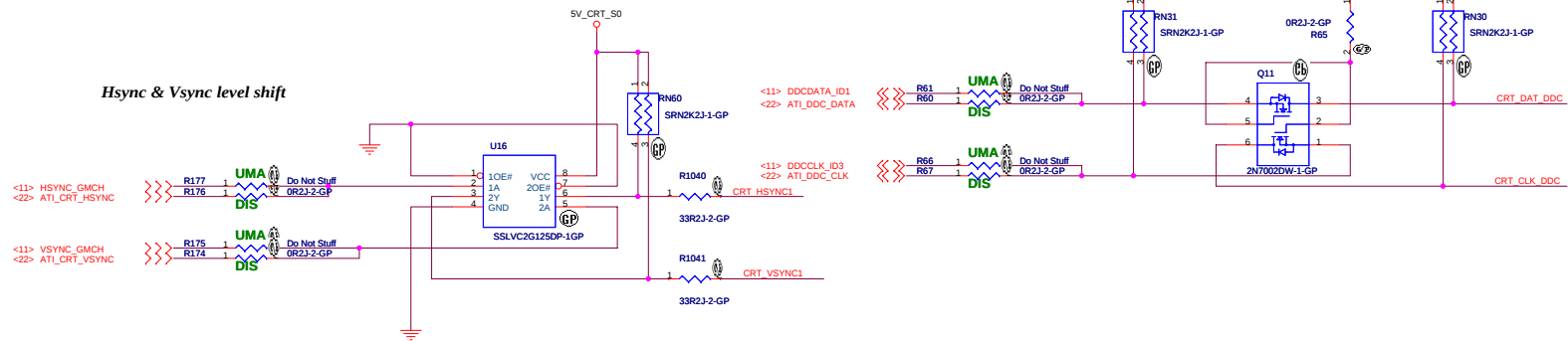
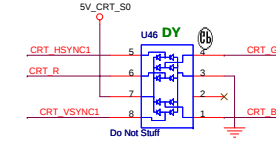
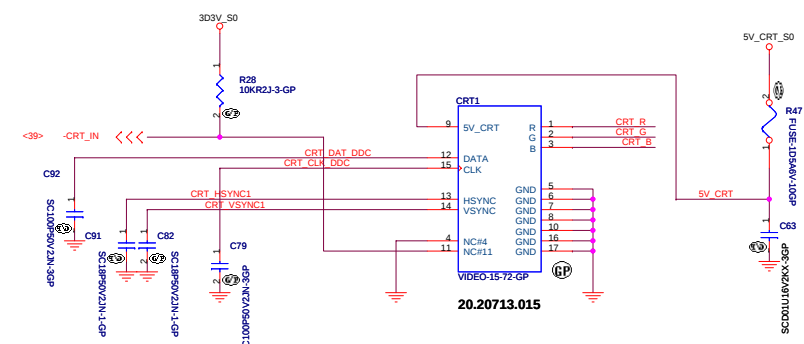
BOM1

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
LCD CONN & CAMERA & DIG-MIC	
Size	Document Number
LT32M	
Date: Monday, July 07, 2008	Sheet 18 of 54

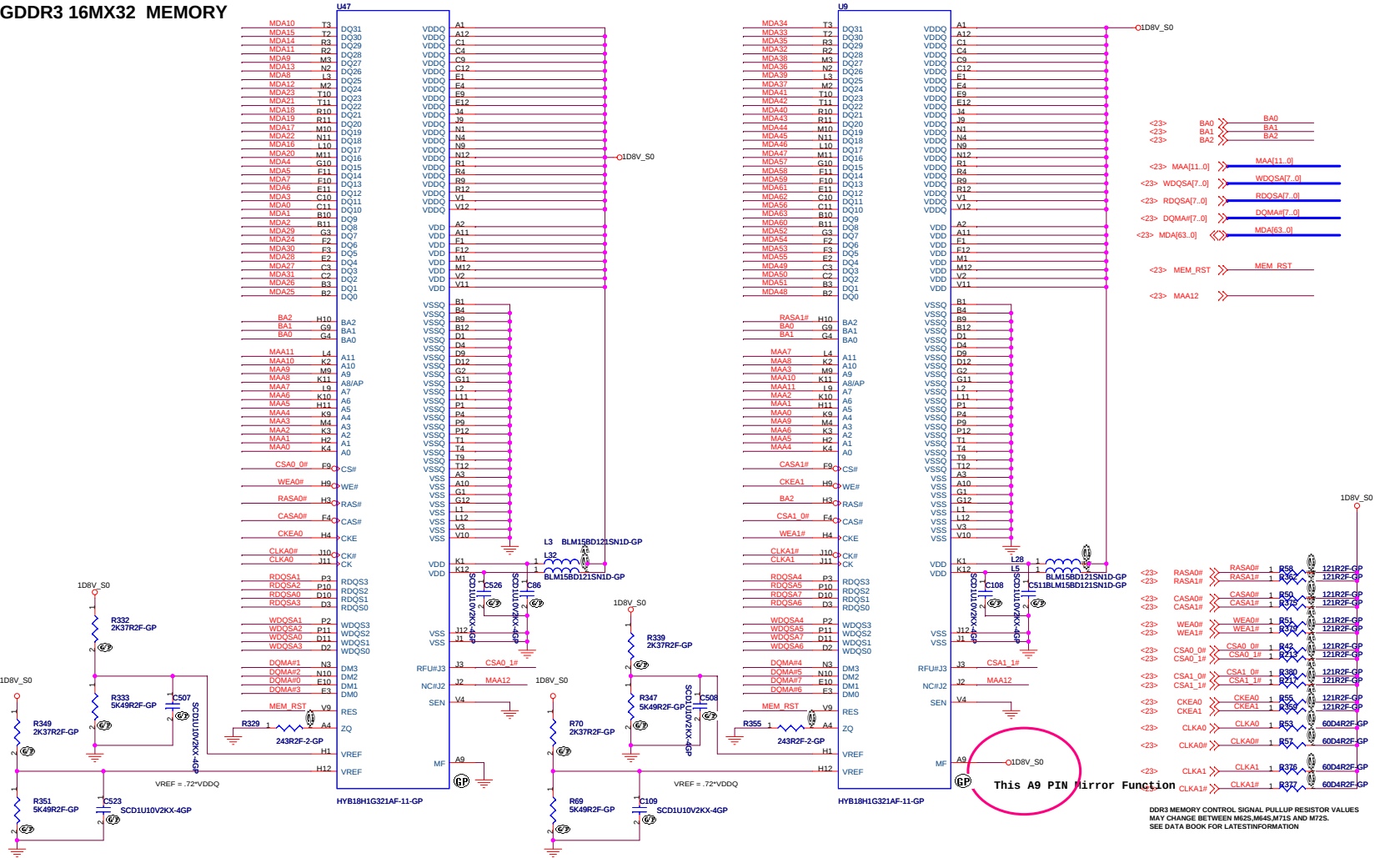
CRT I/F & CONNECTOR



Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



GDDR3 16MX32 MEMORY

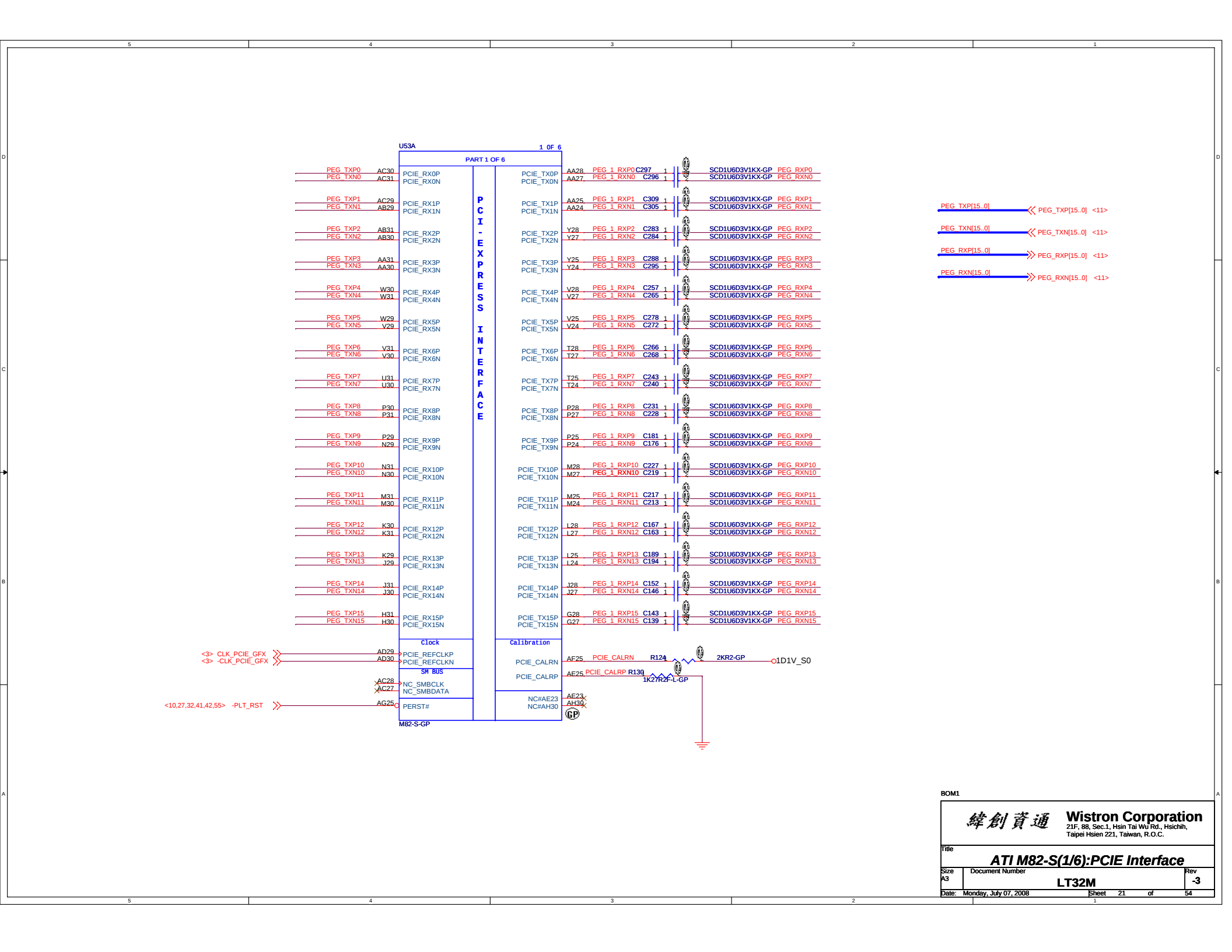


DDR3 MEMORY CONTROL SIGNAL PULLUP RESISTOR VALUES
MAY CHANGE BETWEEN M82S, M82S, M71S AND M72S.
SEE DATA BOOK FOR LATEST INFORMATION

PLACE VREF DIVIDER COMPONENTS
AS CLOSE TO MEMORY AS POSSIBLE

BOM1

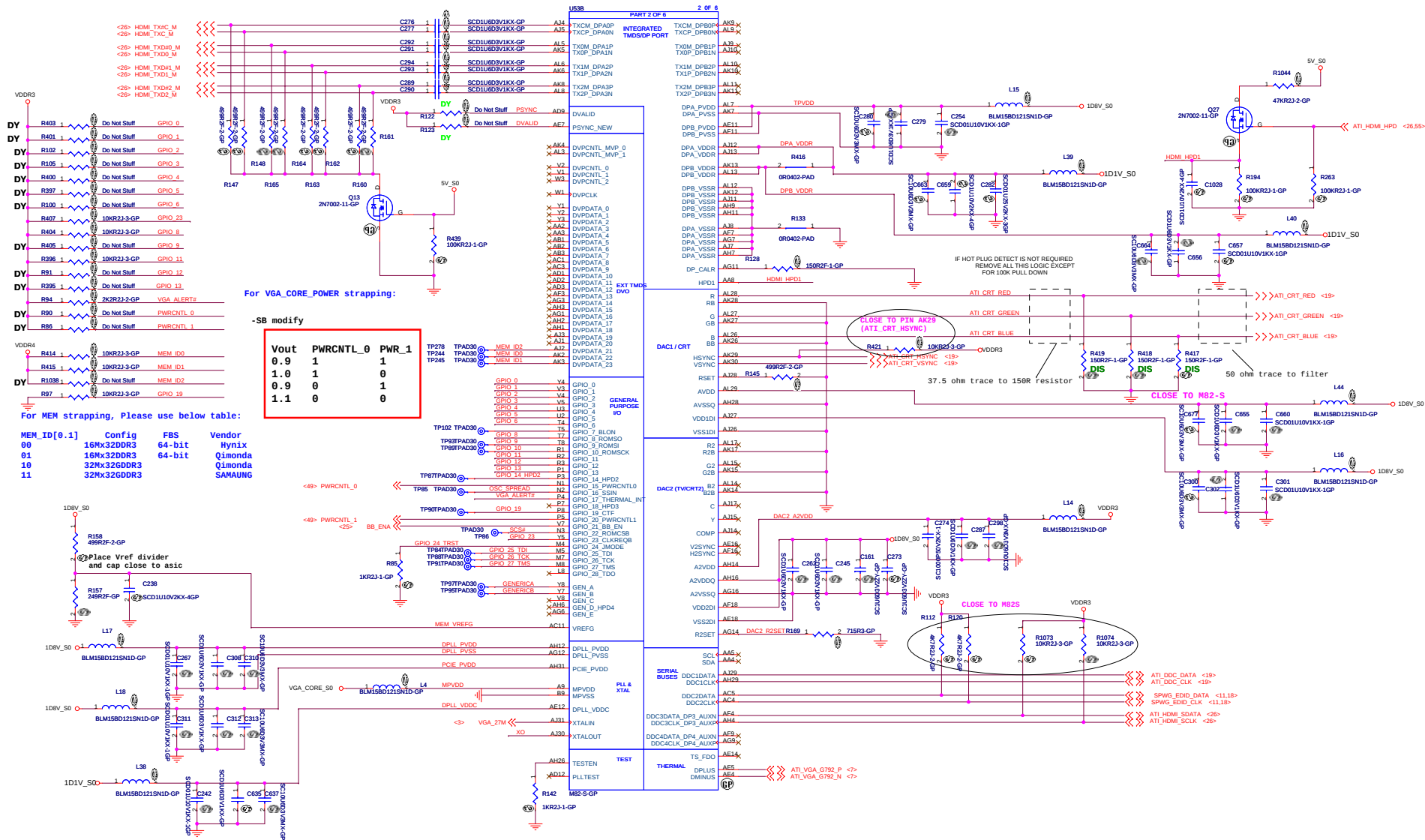
緯創資通 Wistron Corporation		
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.		
Title: ATI M82-S VRAM(1,2)		
Size: C	Document Number: LT32M	Rev: -3
Date: Monday, July 07, 2008		Sheet: 20 of 54



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			ATI M82-S(1/6):PCIE Interface
Size	Document Number	Rev	
A3	LT32M	-3	
Date:	Monday, July 07, 2008	Sheet	21 of 54



For VGA_CORE_POWER strapping:

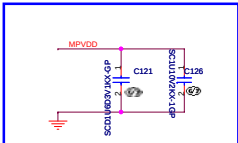
-SB modify

Vout	PWRCNTL_0	PWR_1
0.9	1	1
1.0	1	0
0.9	0	1
1.1	0	0

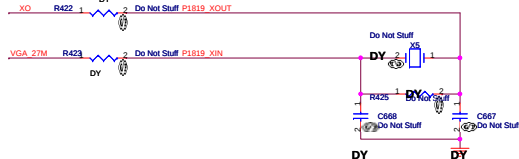
For MEM strapping, Please use below table:

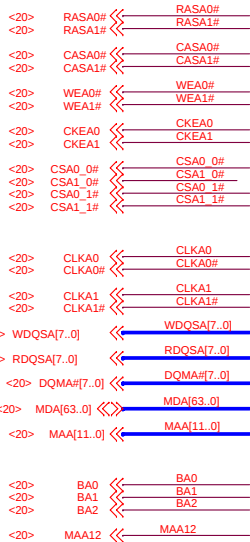
MEM_ID[0..1]	Config	FBS	Vendor
00	16Mx32DDR3	64-bit	Hynix
01	16Mx32DDR3	64-bit	Qimonda
10	32Mx32DDR3		Qimonda
11	32Mx32DDR3		SAMAUNG

P1819B
SRS: 0: -1.25% down spread
1: -1.75% down spread



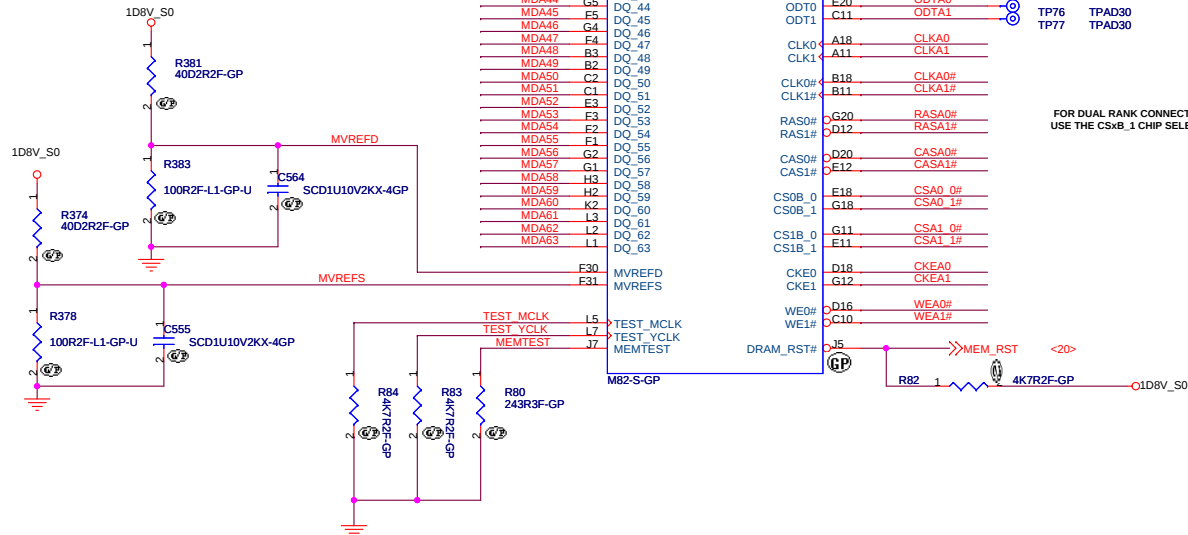
Pls place these capacitors as close to as U14 MPVDD Pin.





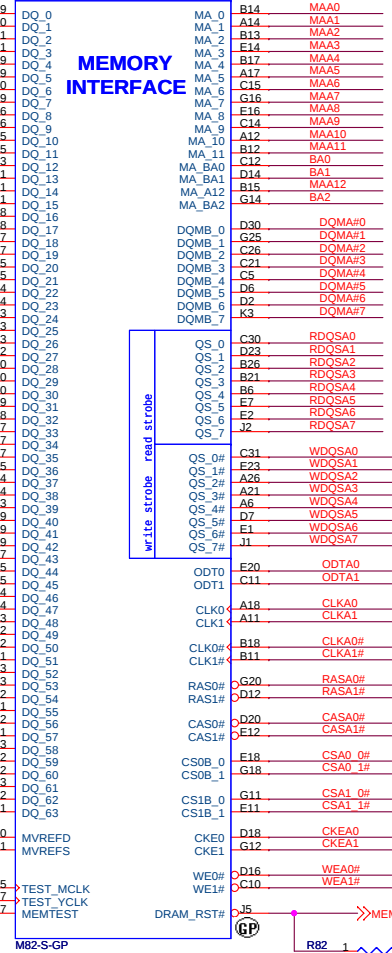
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



U53C 3 OF 6
Part 3 of 6

MEMORY INTERFACE



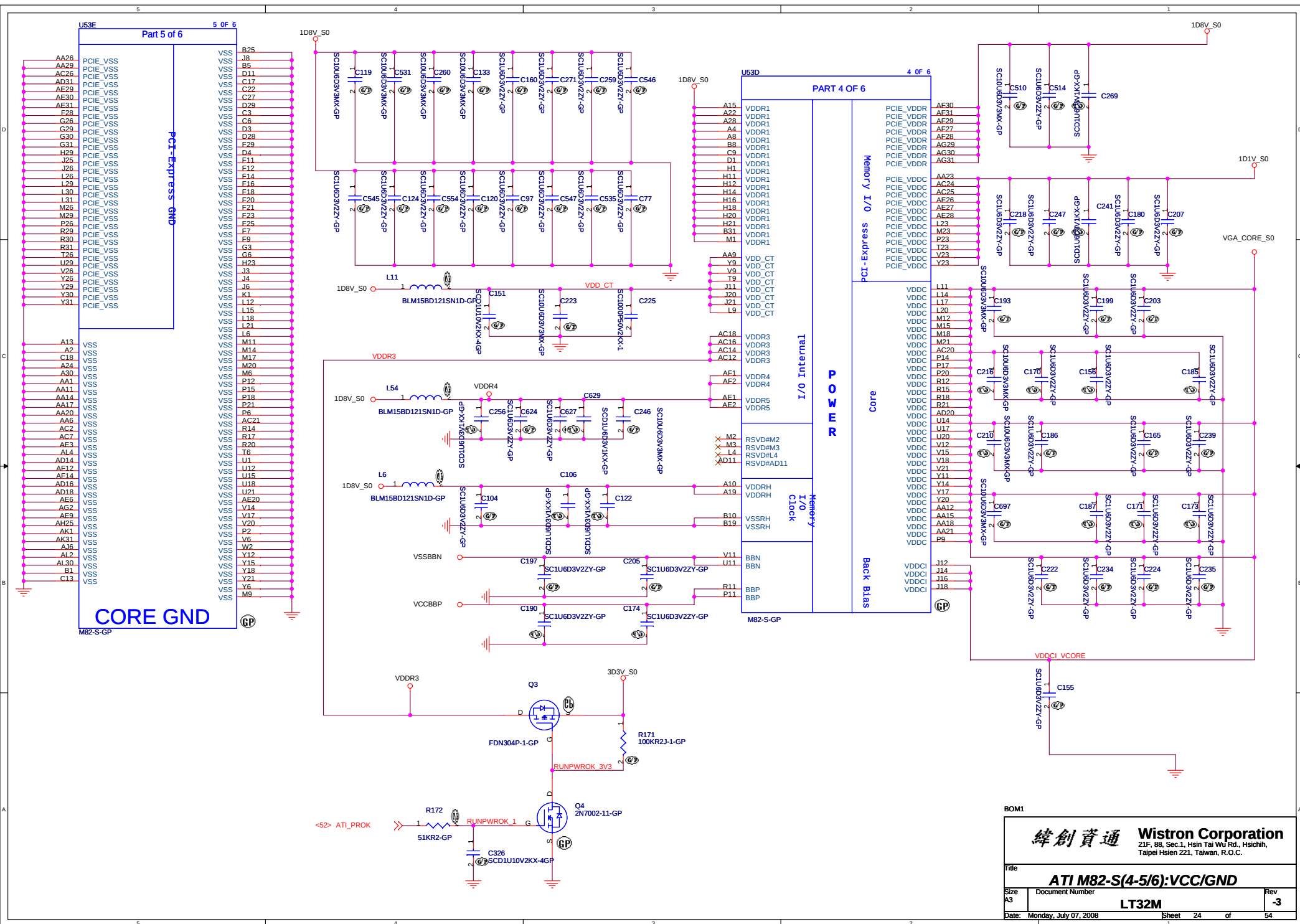
FOR DUAL RANK CONNECTIONS
USE THE CSx8_1 CHIP SELECT PINS

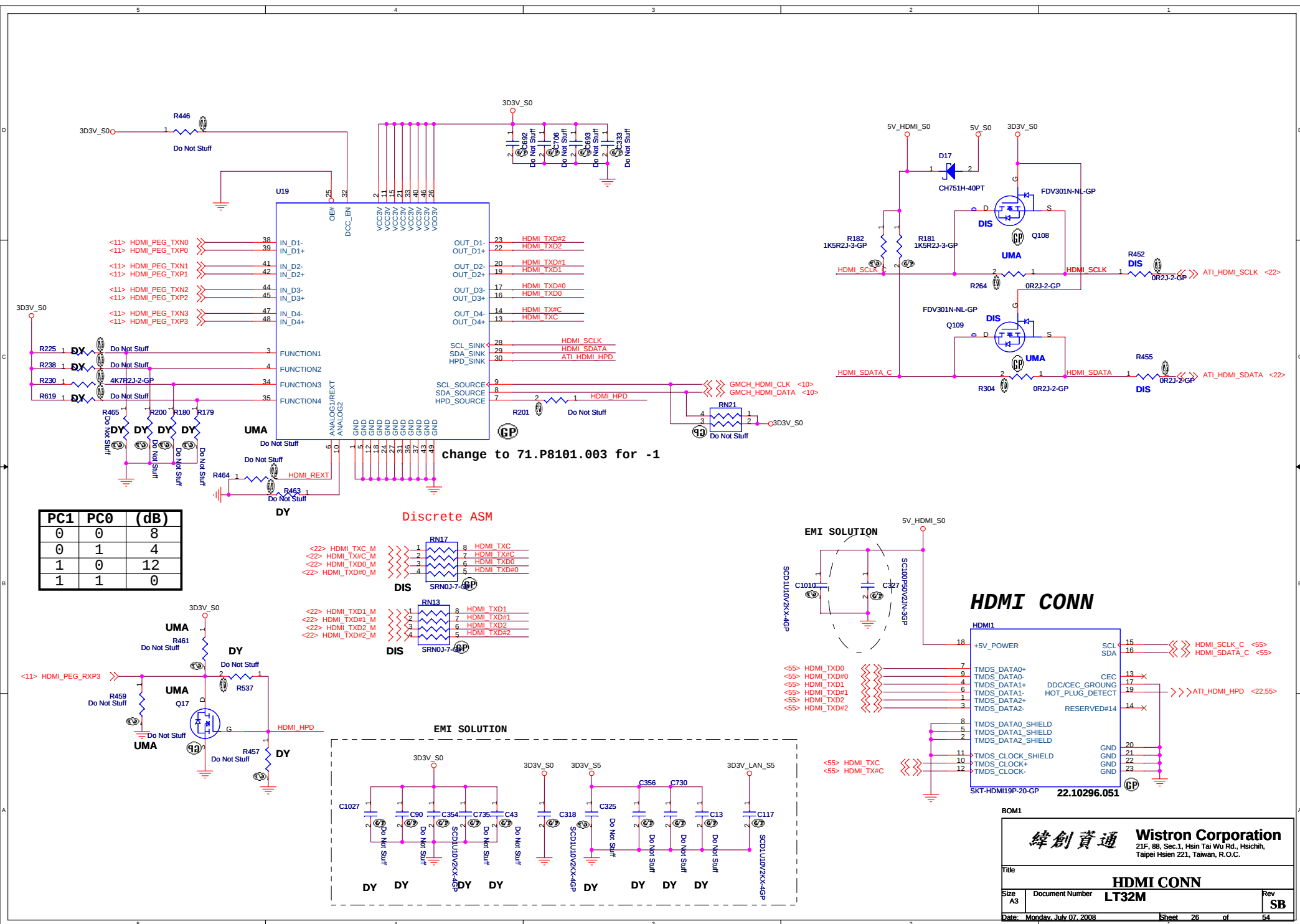
BOM1

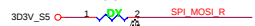
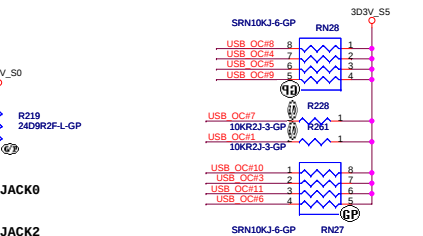
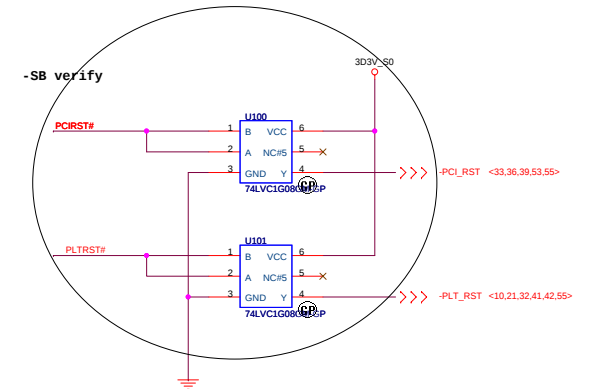
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

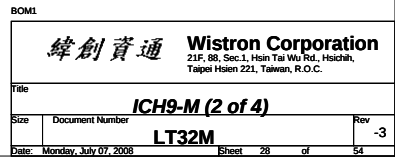
Title **ATI M82-S(3/6):Memory Interface**

Size A3 Document Number **LT32M** Rev **-3**
Date: Monday, July 07, 2008 Sheet 23 of 54









MAIN SOURCE: 20.F0411.003
SECOND SOURCE: 20.D0246.103

20.F0714.003

GLAN_COMP place within 500 mils of ICH9M

<10> ACZ_SDIN
<10> ACZ_SDOOUT
<10> ACZ_SYNC
<10> -ACZ_RST
<10> ACZ_BITCLK

Do Not Stuff
Do Not Stuff

<40,55> ACZ_BITCLK_MDC
<35> ACZ_BITCLK_RTL
<35> ACZ_SYNC_RTL
<40,55> ACZ_SYNC_MDC
<40,55> -ACZ_RST
<35> -ACZ_RST_MDC
<35> -ACZ_RST_RTL

<35> ACZ_SDATIN_RTL
<40,55> ACZ_SDATIN_MDC

<40,55> ACZ_SDATOUT_RTL
<35> ACZ_SDATOUT_MDC

<53> SATA_LED#
<32,55> SATA_RXN0
<32,55> SATA_RXP0
<32,55> SATA_TXN0
<32,55> SATA_TXP0
<32,55> SATA_RXN1
<32,55> SATA_RXP1
<32,55> SATA_TXN1
<32,55> SATA_TXP1

KDS: RESO 32.768KHZ / 12P

U24A 1 OF 6

RTC

LPC

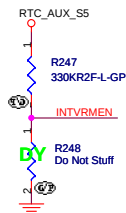
LAN / GLAN

CPU

IHDA

SATA

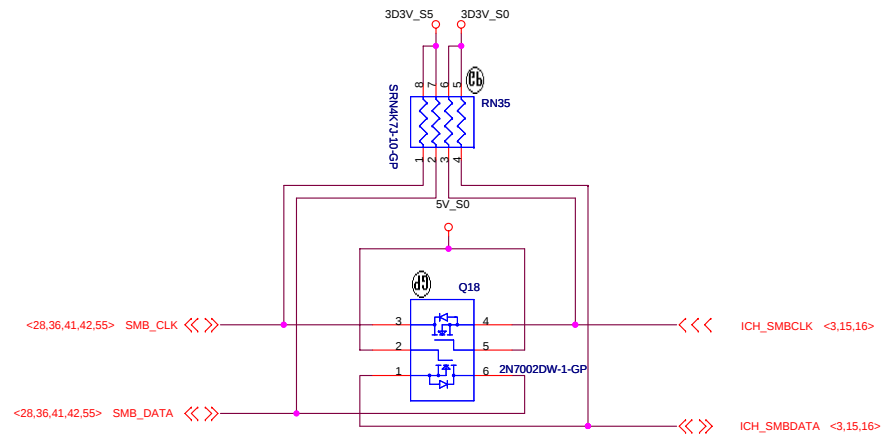
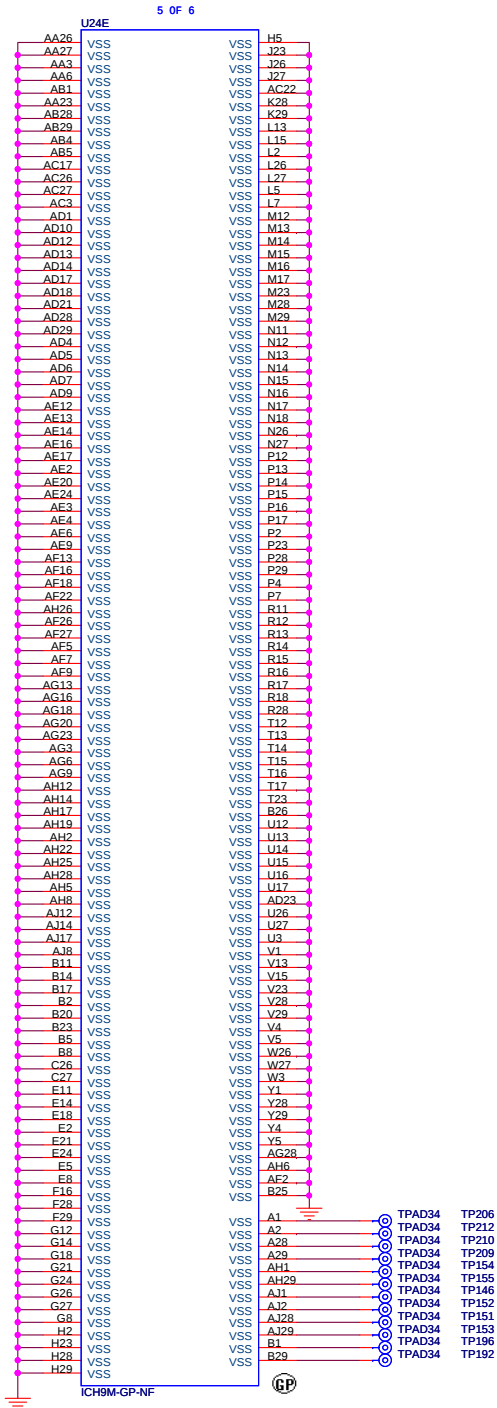
ICH9M-GP-NF



Integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
Integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

BOM1

緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title ICH9-M (1 of 4)	
Size	Document Number
Date: Monday, July 07, 2008	LT32M
Sheet 29	Rev -3

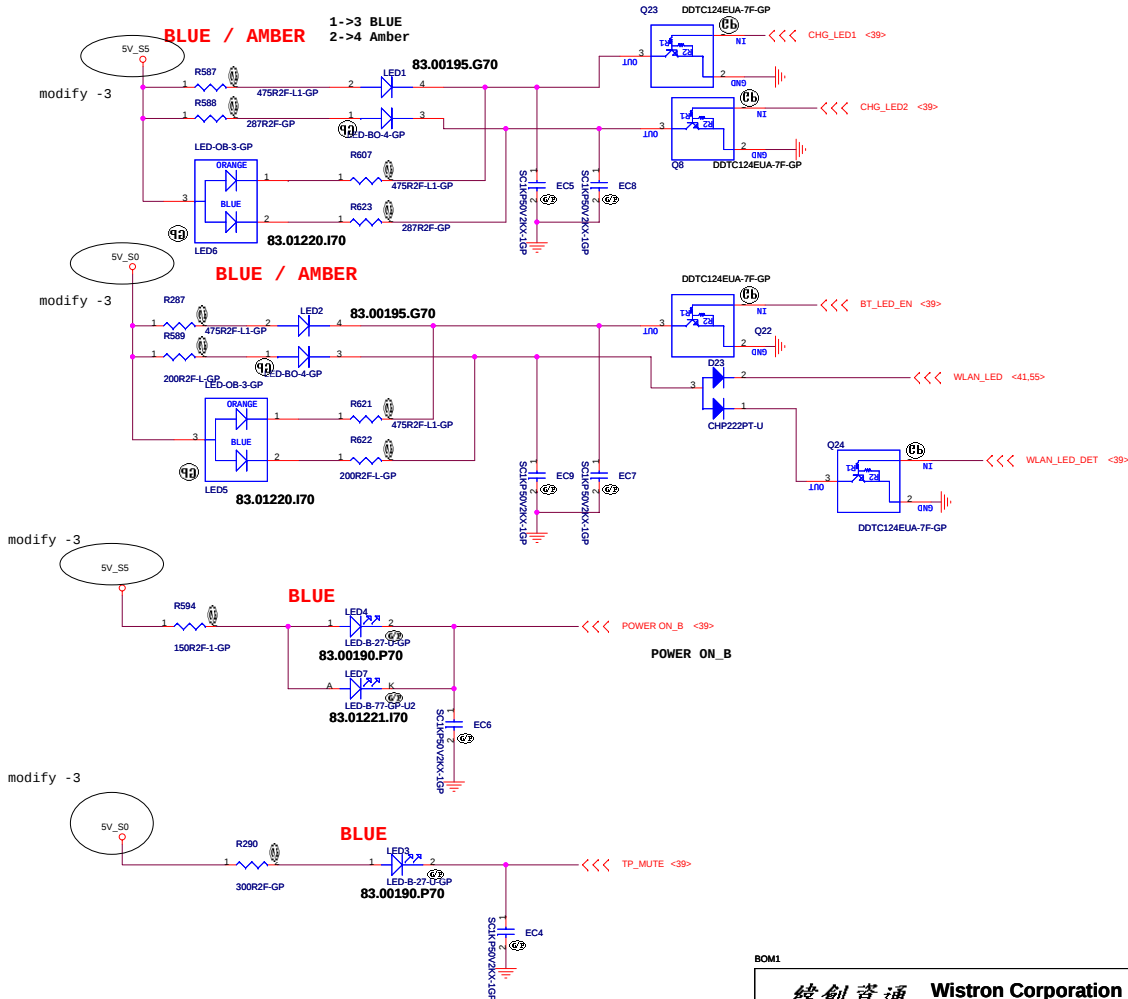
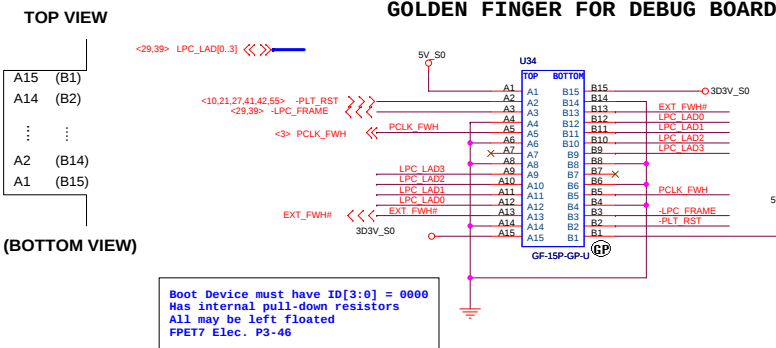
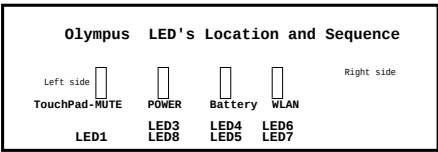
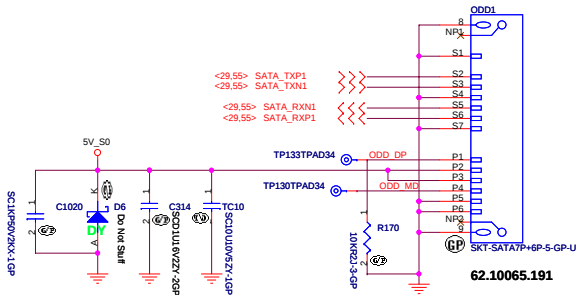
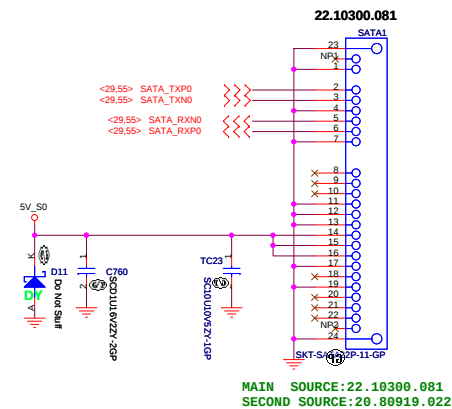


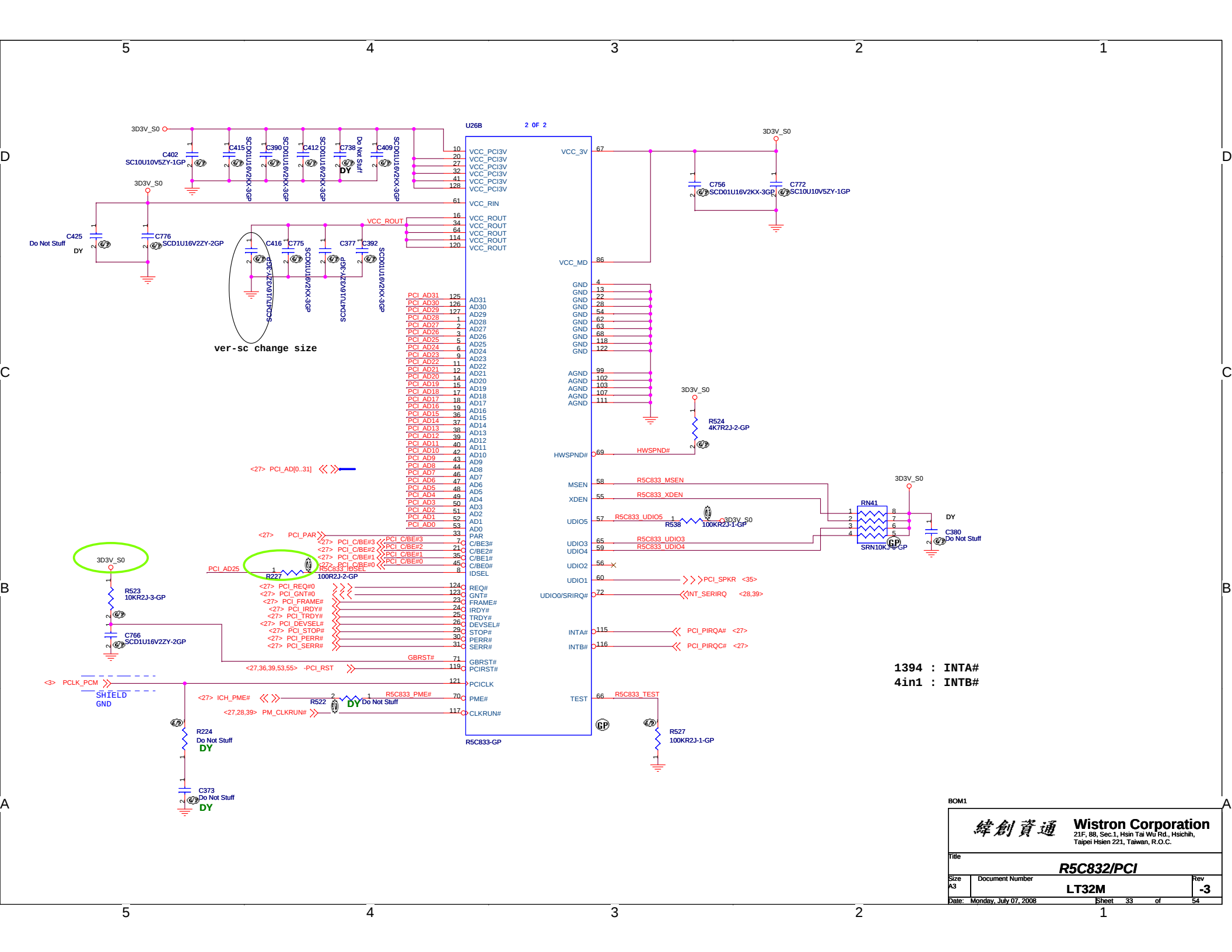
Q13 & Q14 connect SMLINK and
SMBUS in S) for SMBus 2.0
compliance

SMBUS

SATA HD Connector

ODD Connector





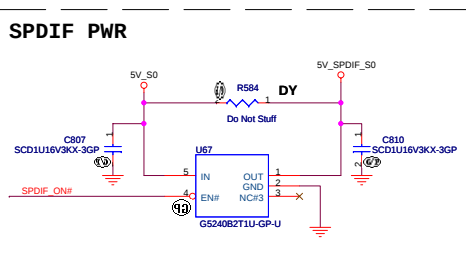
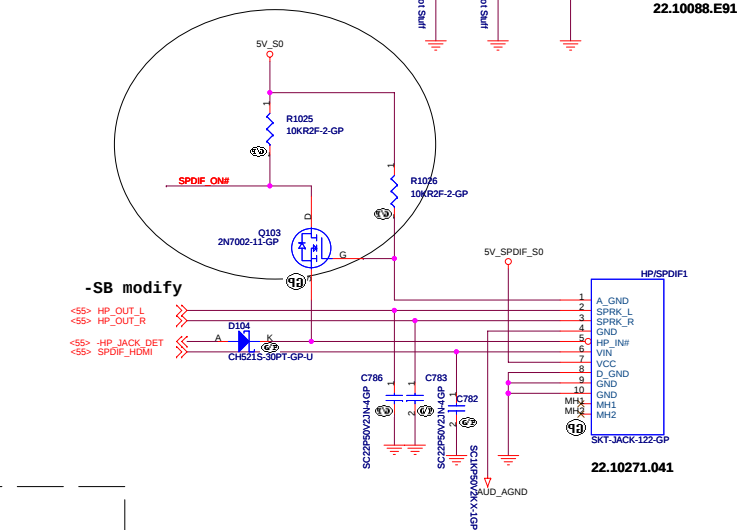
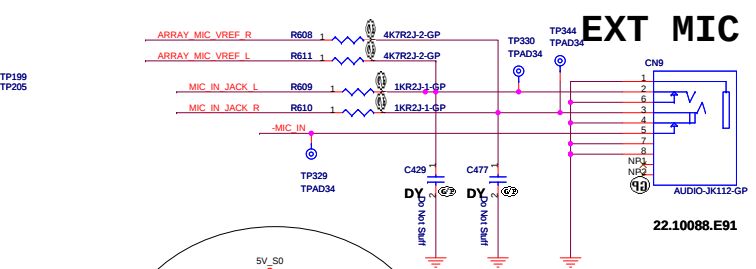
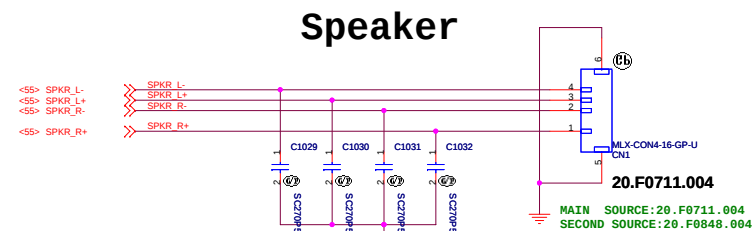
1394 : INTA#
4in1 : INTB#

BOM1

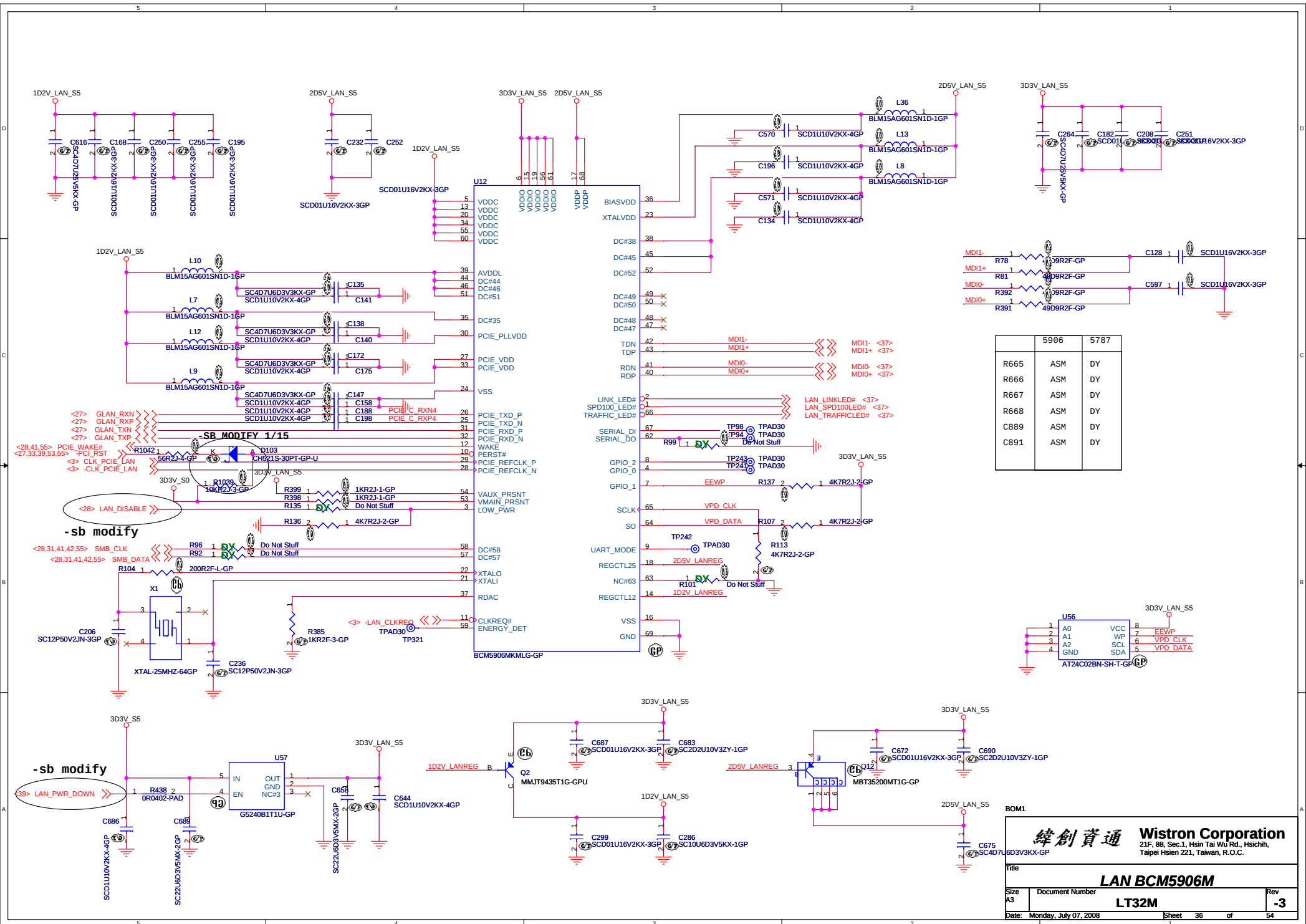
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
R5C832/PCI		
Size	Document Number	Rev
A3	LT32M	-3
Date:	Monday, July 07, 2008	Sheet 33 of 54



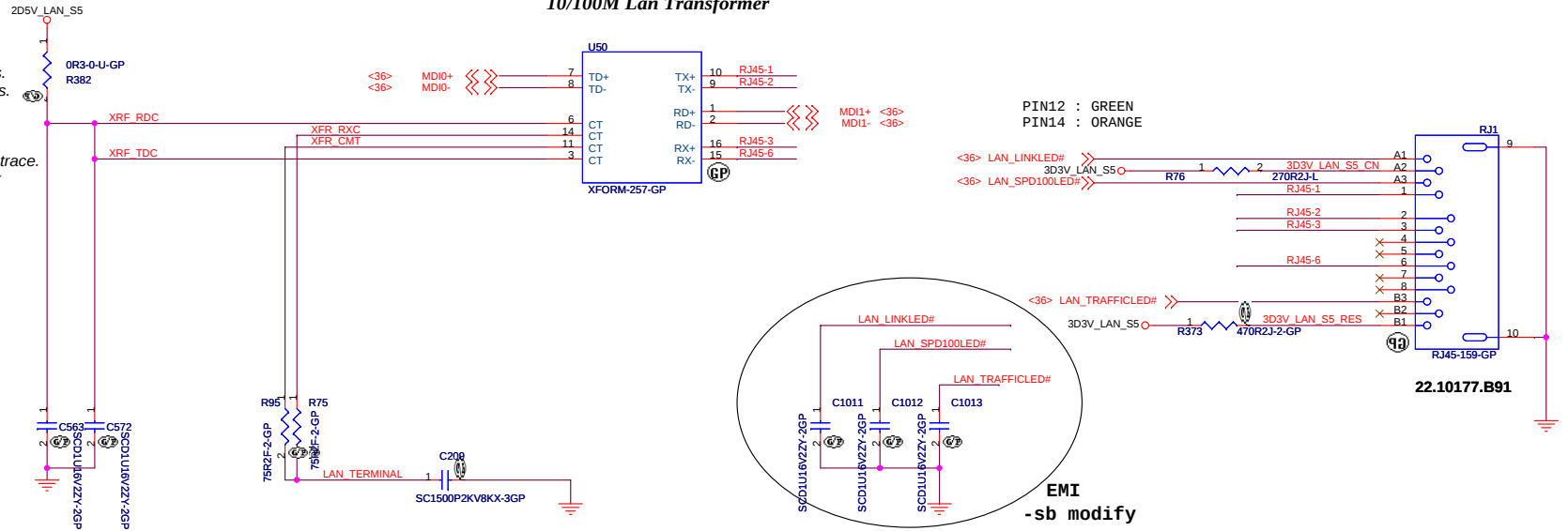


HP_OUT/ LINE_OUT



10/100M Lan Transformer

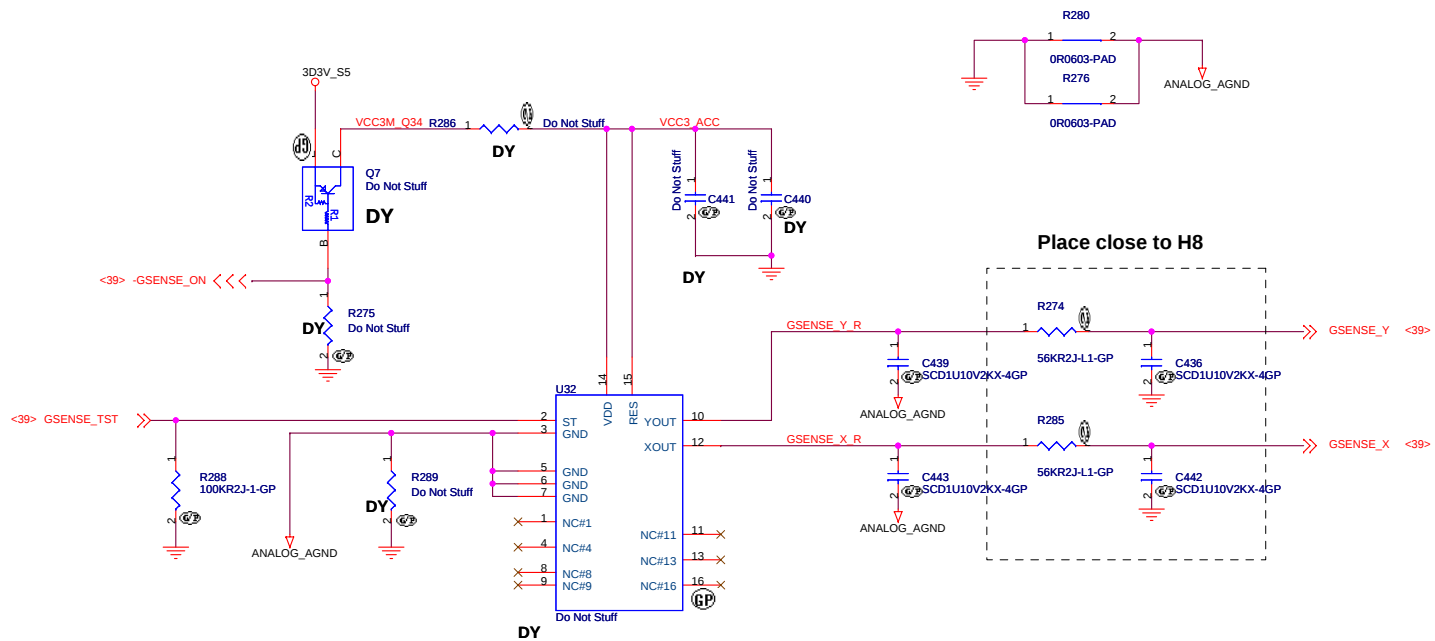
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.



BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
LAN connector/NEW CARD/SIM			
Size	Document Number	Rev	
A3	LT32M	-3	
Date: Monday, July 07, 2008		Sheet 37 of 54	



Primary : STMicro LIS244AL
2nd: ADI ADXL322

Width = 6 mil & Spacing = 10 mil
for three Output traces

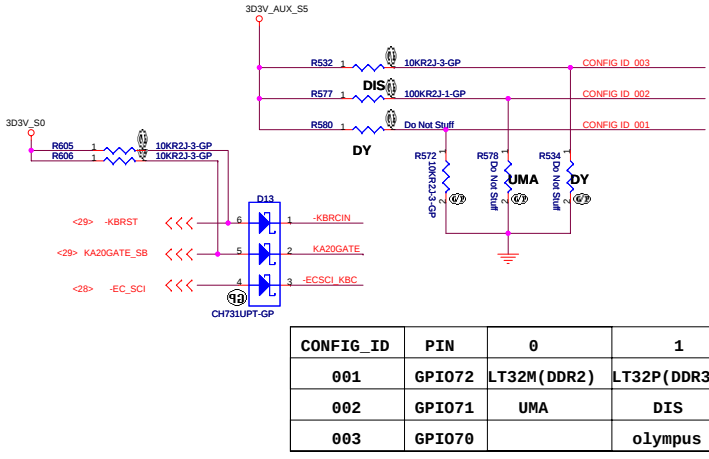
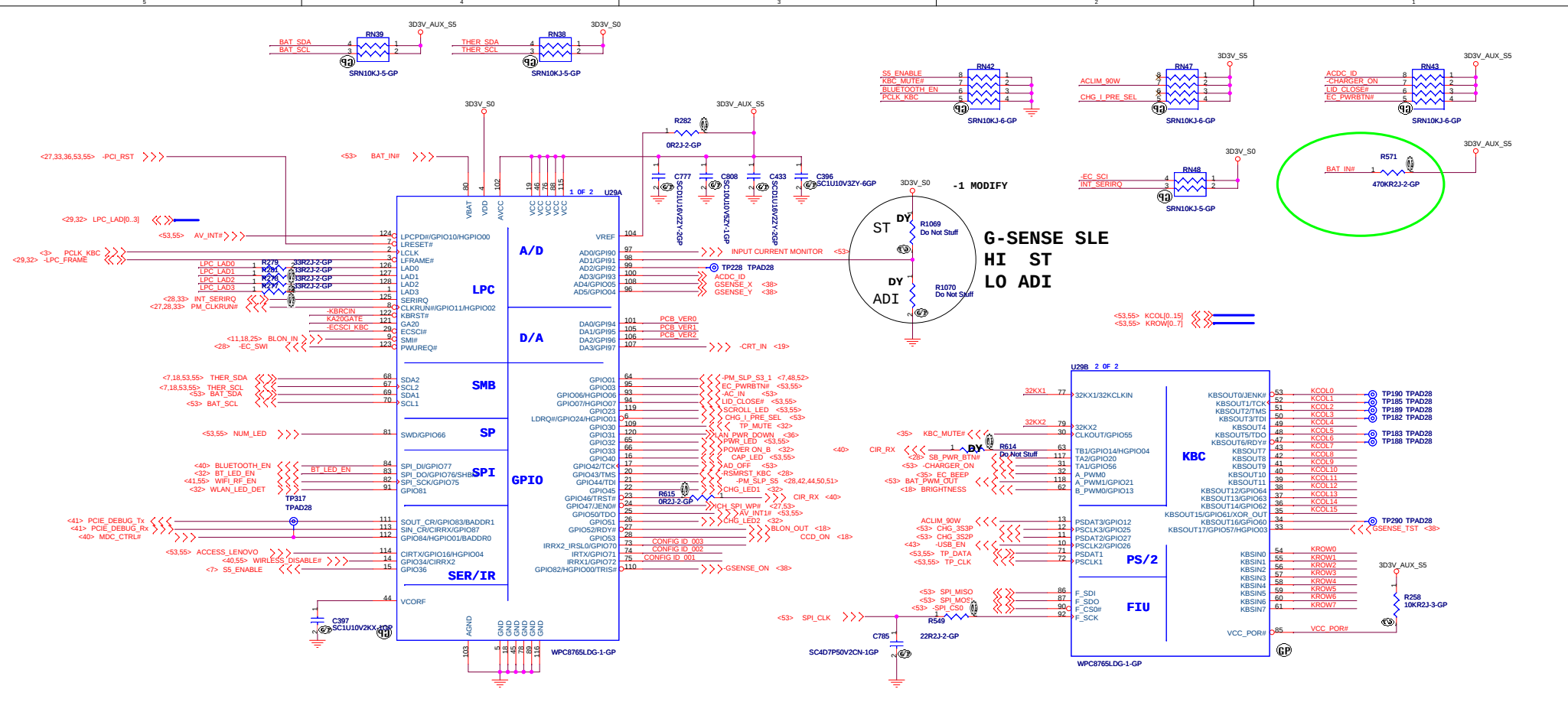
	ADXL322 LIS244AL	No Accel
R545	NO_ASM	ASM
R547	ASM	ASM
All other	ASM	NO_ASM

Layout Comment :

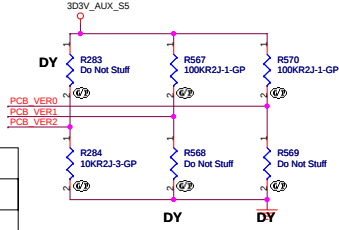
- (1) Place C439, C443, Q7, R286, R275, C441, C440, R288, R289 close to U32.
- (2) Avoid routing under DCDC switching area.

BOM1

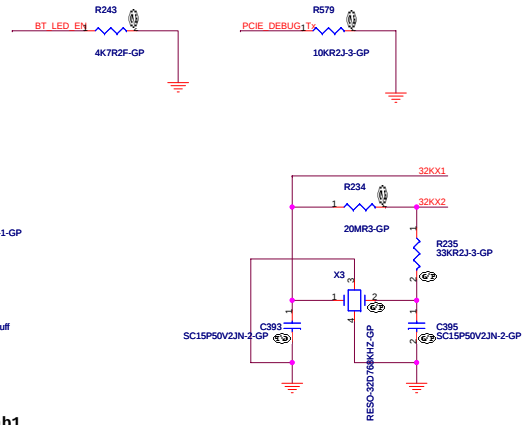
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
G-SENSOR		
Size A3	Document Number LT32M	Rev -3
Date: Monday, July 07, 2008	Sheet 38 of 54	

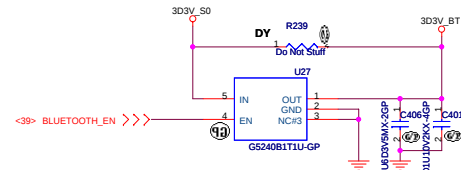


CONFIG_ID	PIN	0	1
001	GPI072	LT32M(DDR2)	LT32P(DDR3)
002	GPI071	UMA	DIS
003	GPI070		olympus



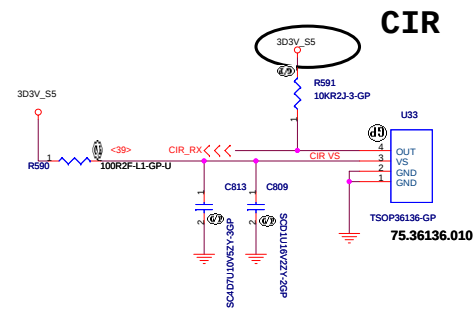
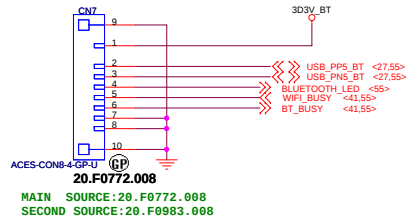
PID_LAB1 = 000b ; Lab1
 PID_LAB2 = 001b ; Lab2
 PID_ENG = 010b ; ENG
 PID_PD = 011b ; PD





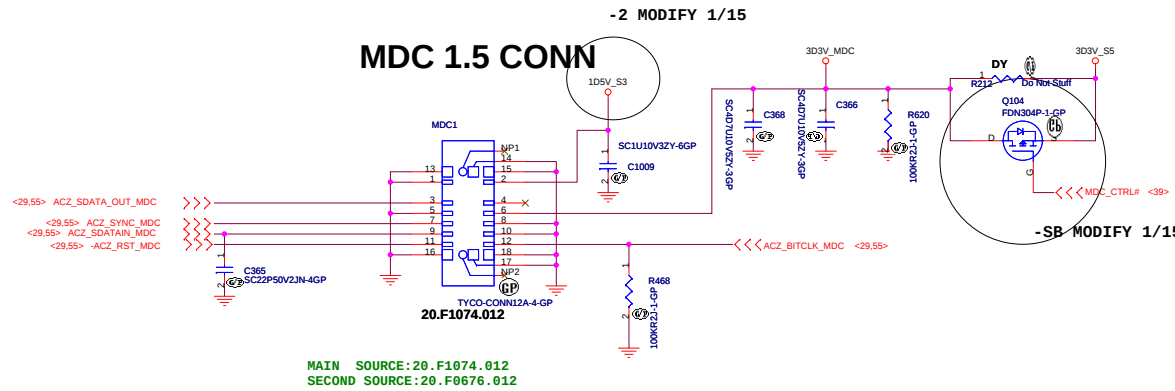
SB

BT CONNECTOR

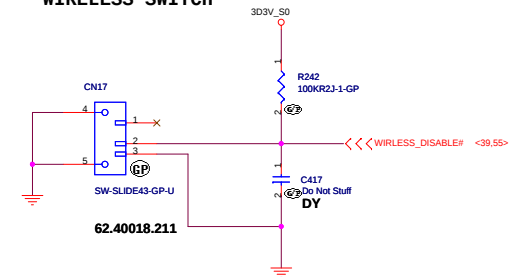


CIR

MDC 1.5 CONN



WIRELESS SWITCH



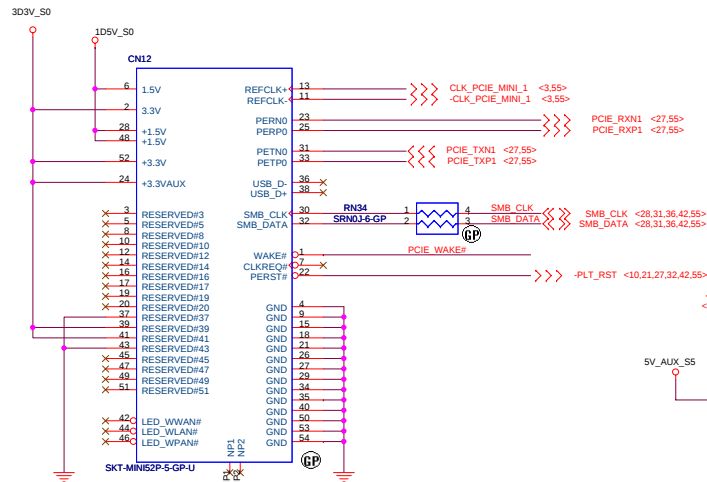
BOM1

Mini PCI-E Connector

Only port-1 support USB

For Robson

Port-1 High

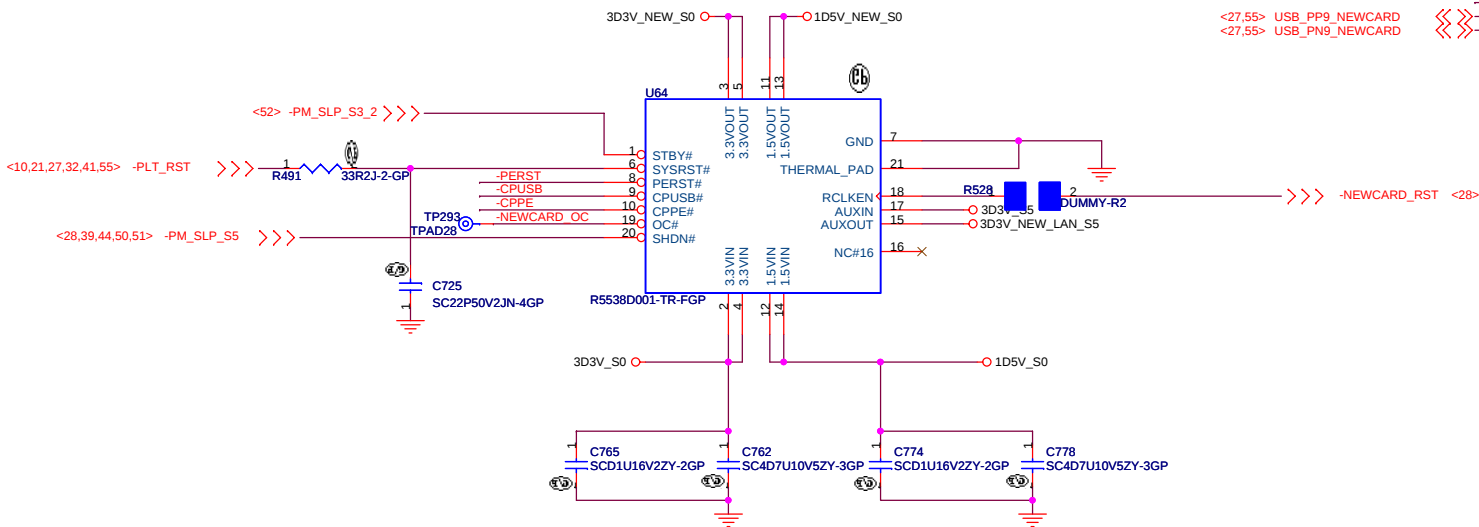
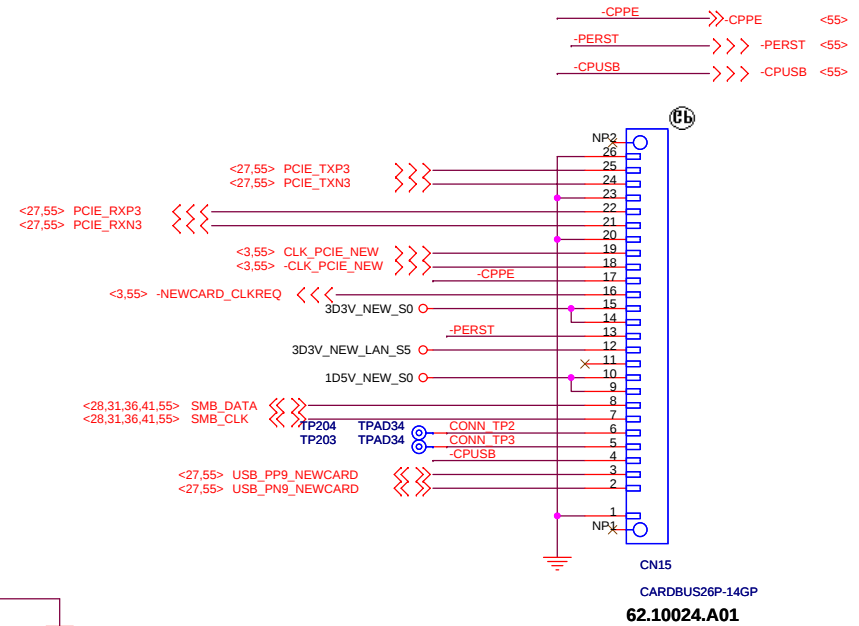
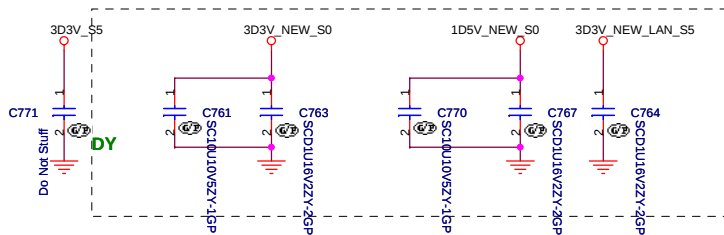


NEWCARD Connector

For Newcard socket

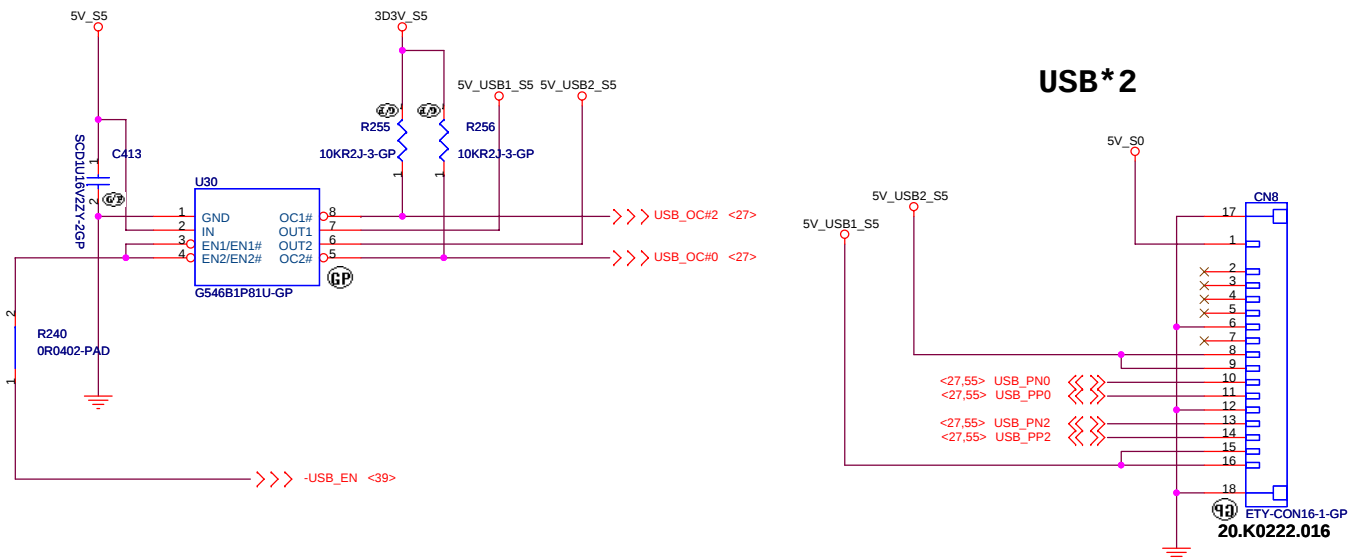
Place them Near to Chip

Place them Near to Connector



BOM1

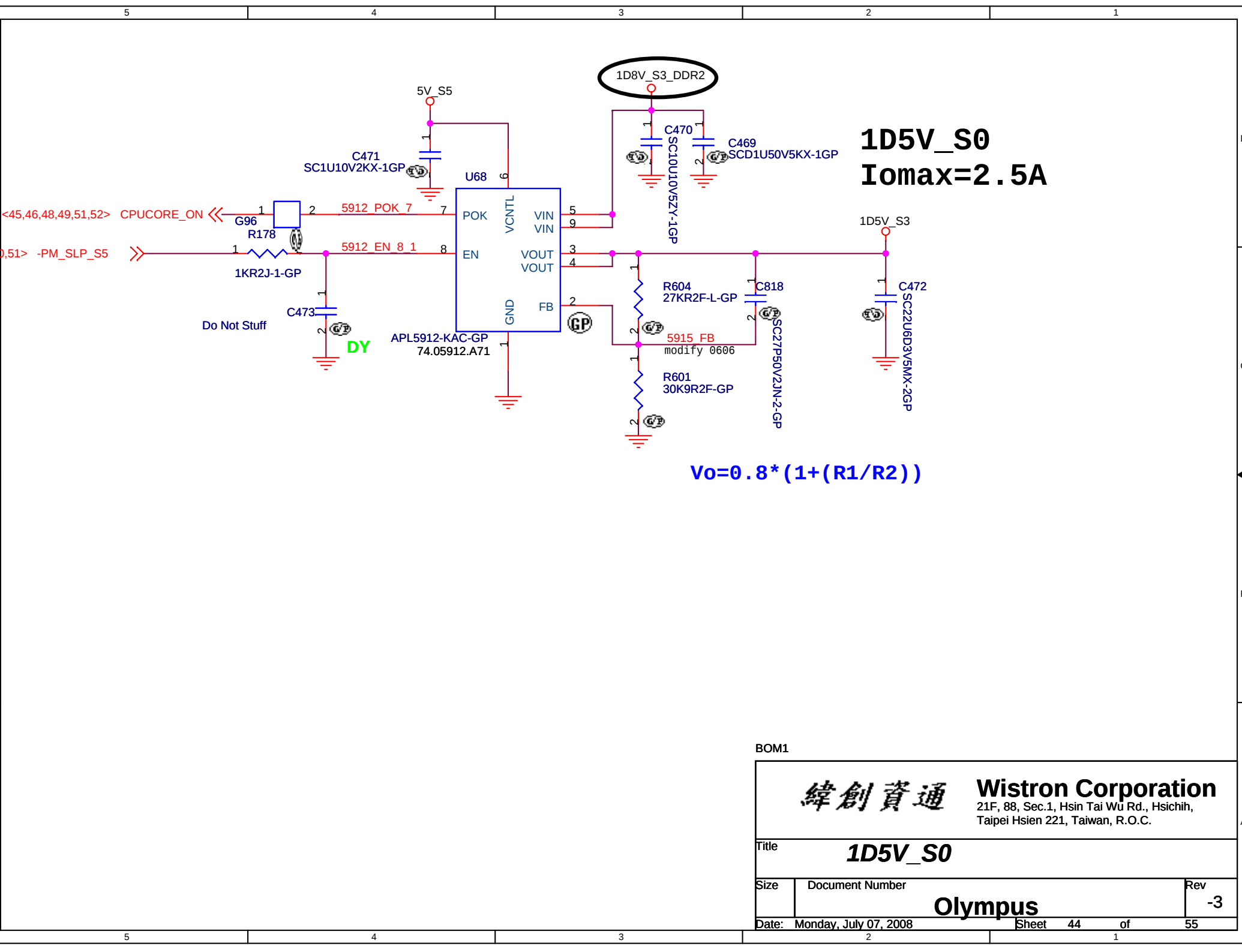
緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		Title	
Size		Document Number	
Date: Monday, July 07, 2008		Sheet 42 of 54	
Module NewCard		Rev -3	
LT32M		BOM1	

[illegible]

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
USB I/O & 1394 CNN			
Size B	Document Number		Rev
	LT32M		-3
Date:	Monday, July 07, 2008	Sheet 43 of	54

D
C
B
A



BOM1

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
1D5V_S0

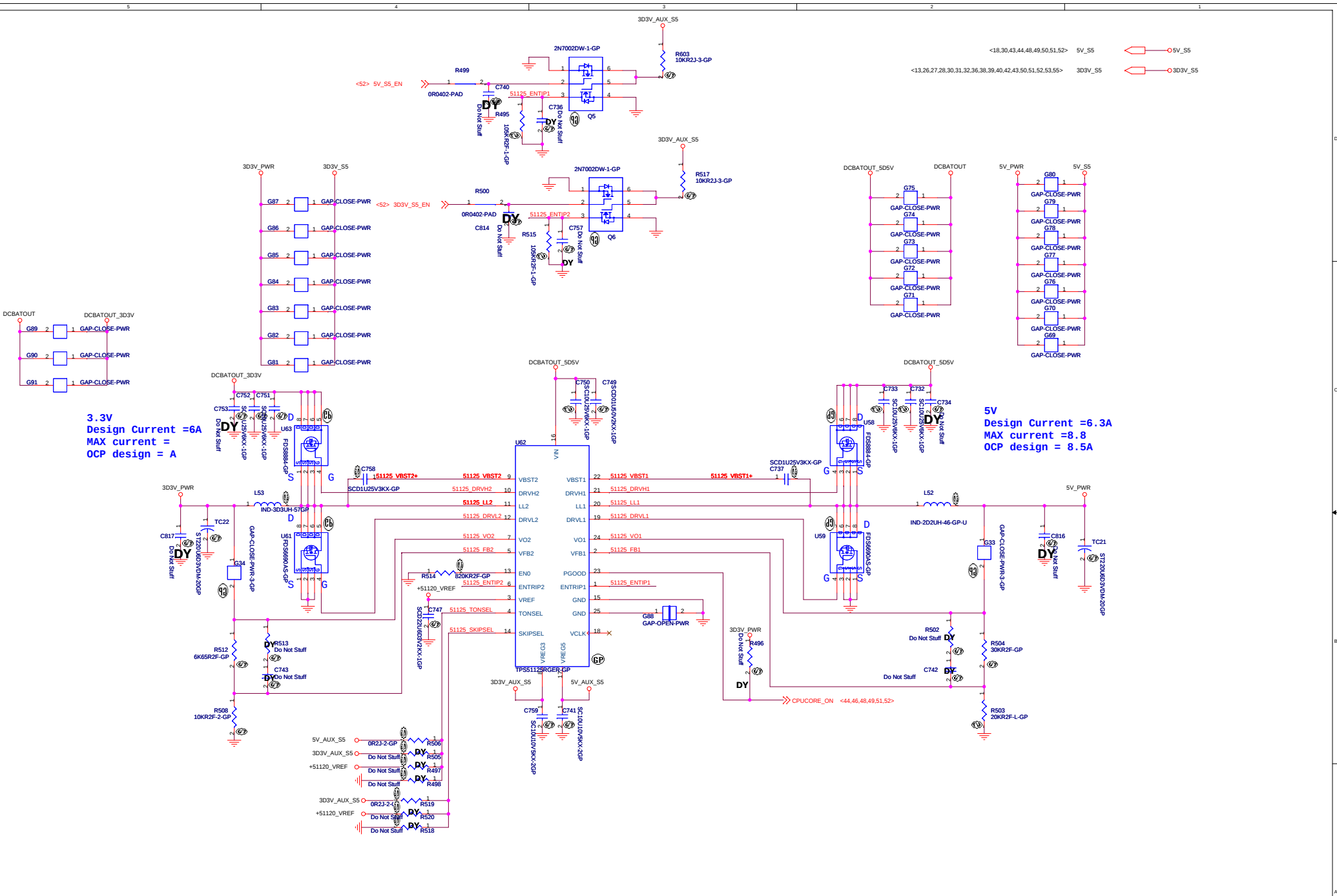
Size Document Number

Olympus

Rev
-3

Date: Monday, July 07, 2008

Sheet 44 of 55



3.3V
Design Current =6A
MAX current =
OCP design = A

5V
Design Current =6.3A
MAX current =8.8
OCP design = 8.5A

-SC MODIFY 1/15

<10.28> PM_DPRSLPVR
<4.10.29> -DPRSTP
<10.28> -VGAET_PWRG

-1 MODIFY

-1 MODIFY

sc-modify

Iomax: 38A

CPU noise

Place close to 1st phase choke

-1 MODIFY

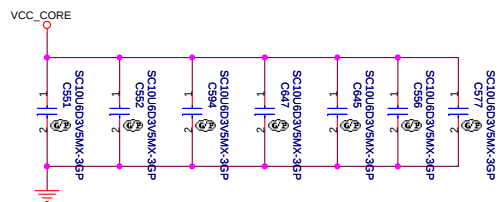
-1 MODIFY

Place close to 1st Choke

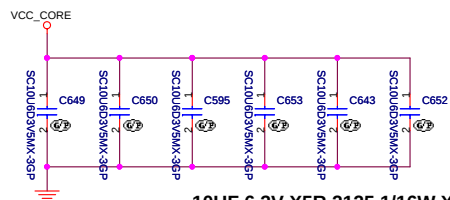
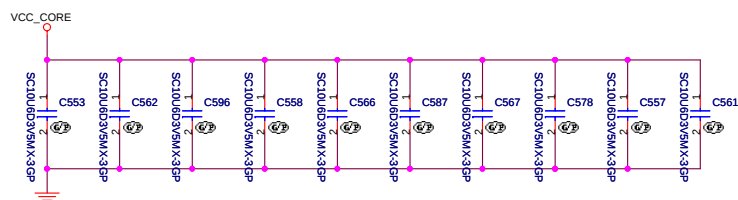
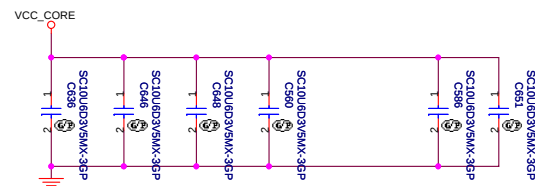
BOM1

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsien 221, Taiwan, R.O.C.

File			
ISL6266A_CPU_CORE			
Size			
Document Number	LT32M	Rev	-3
Date			
Monday, July 07, 2008	Sheet 46	of	55



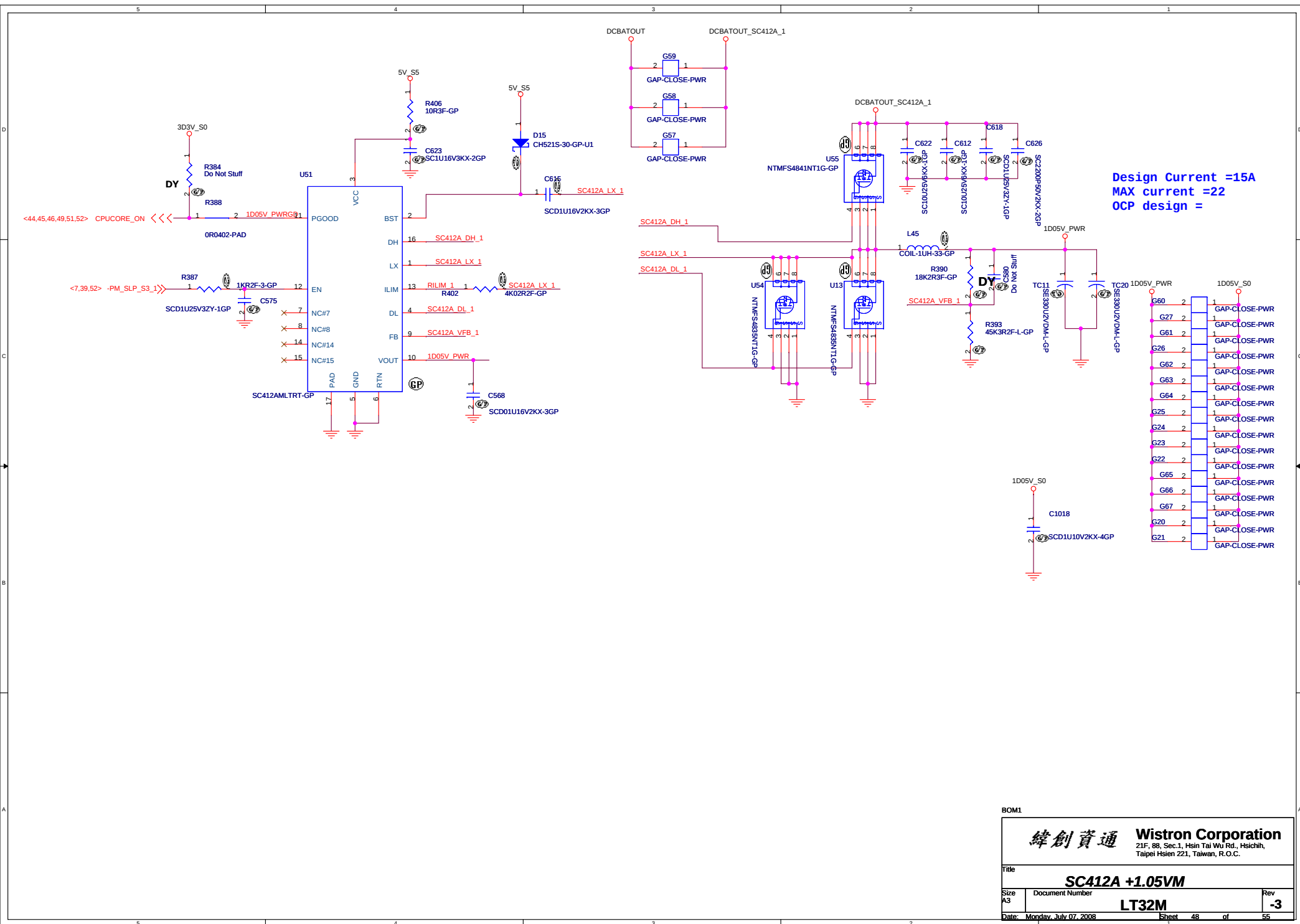
10UF 6.3V X5R 2125 1/16W X16 PCS

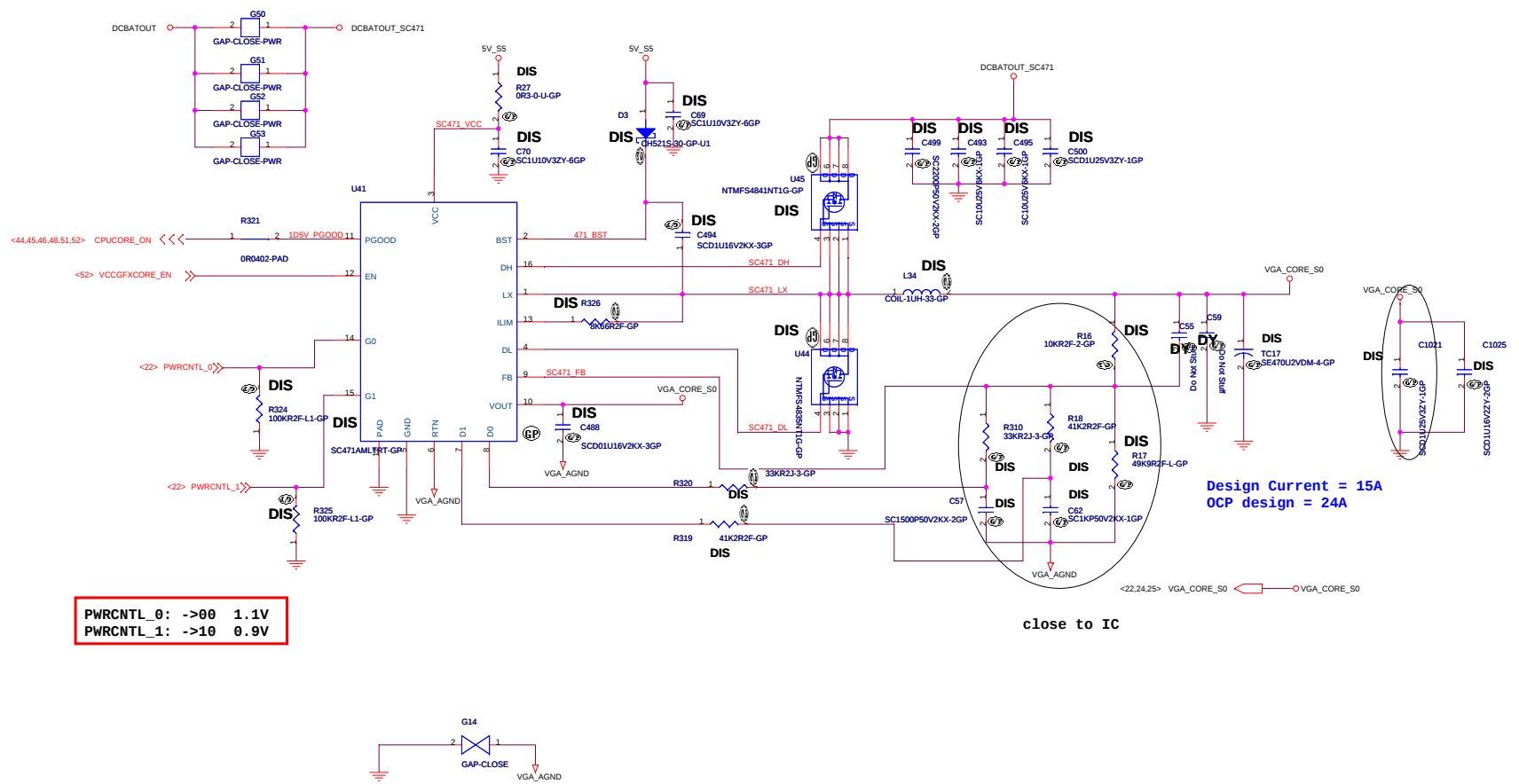


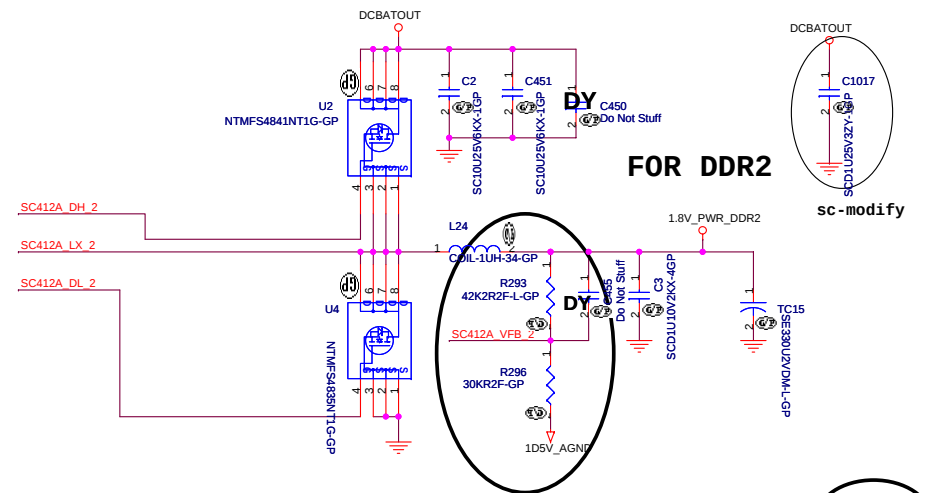
10UF 6.3V X5R 2125 1/16W X16 PCS

BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File	VCCCPUCORE DECOUPLING		
Size	Document Number	Rev	
Custom	LT32M	-3	
Date:	Monday, July 07, 2008	Sheet	47 of 55





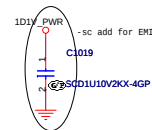
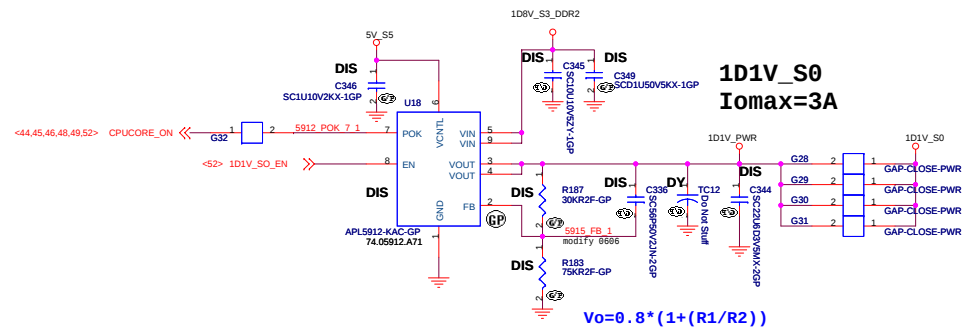
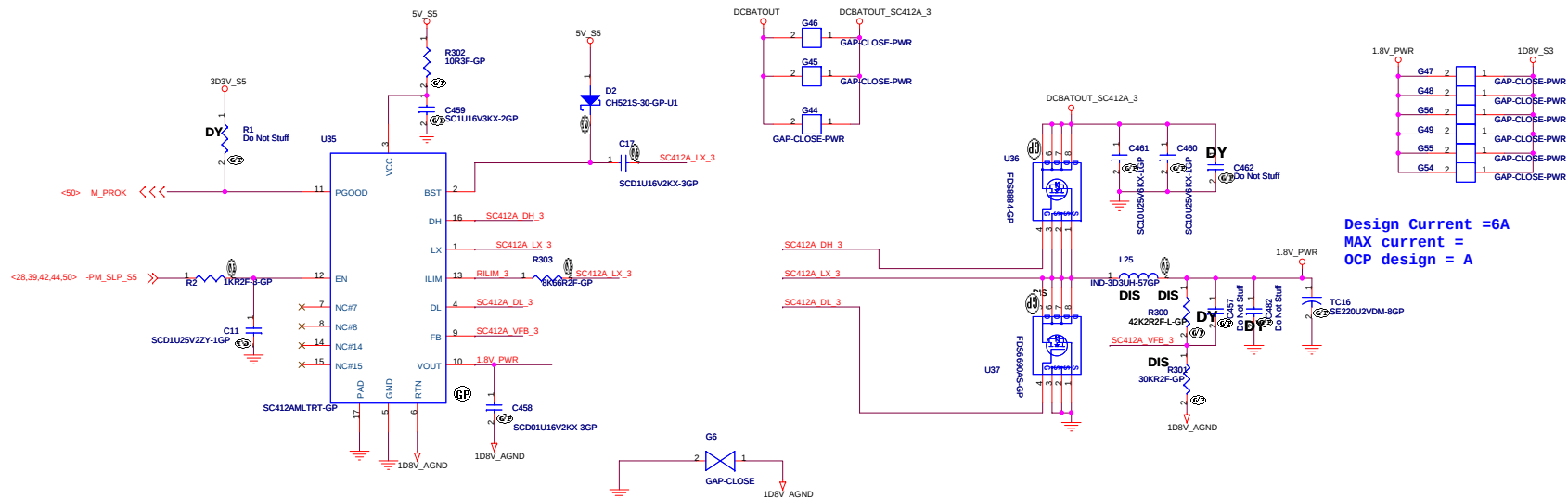


Timing diagram showing signals 1.8V_PWR_DDR2 and 1D8V_S3_DDR2. The diagram includes a table of signal names and their corresponding values, and a visual representation of the signals over time.

Signal Name	Value
G39	1
G40	2
G5	2
G42	2
G1	2
G43	2
G2	2
G3	2
G4	2

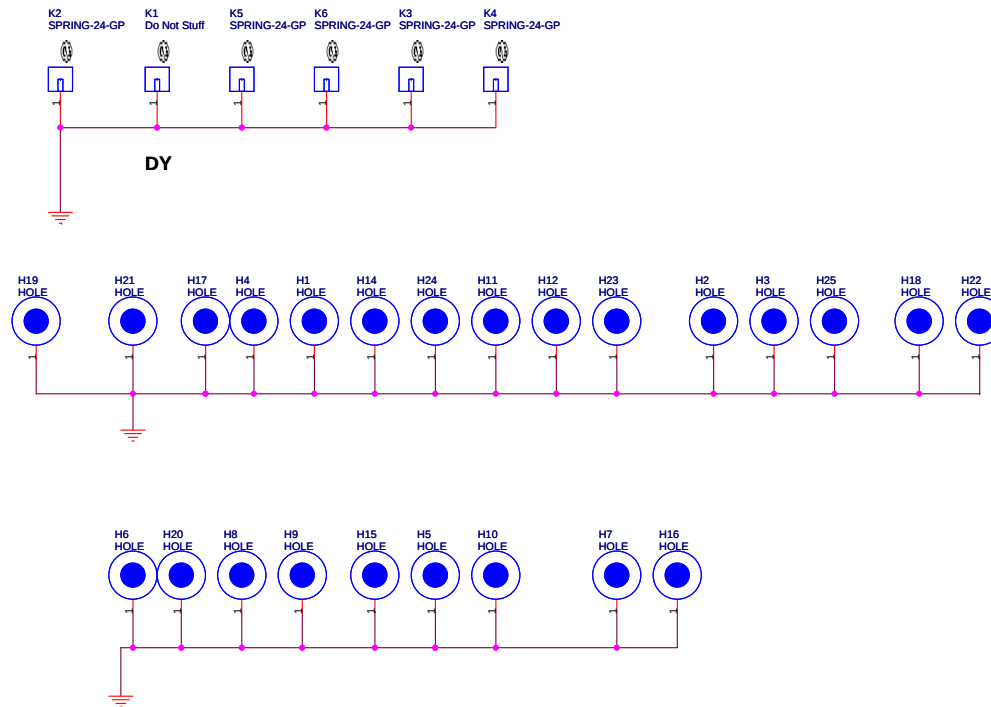
The visual representation shows the signals 1.8V_PWR_DDR2 and 1D8V_S3_DDR2. The 1D8V_S3_DDR2 signal is circled in red.





BOM1

緯創資通		Wistron Corporation	
		21F, 80, Sec.1, Hsin Tai Wu Rd., Hsichai, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
SC412A 1.8V/1.1V			
Size	Document Number	Rev	
	LT32M	-3	
Date: Monday, July 07, 2008	Sheet 51	of	55



BOM1

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File PTH FOR SCREW HOLES			
Size	Document Number	Rev	
Custom	LT32M	-3	
Date: Monday, July 07, 2008	Sheet 54	of 55	

